

Z0103MN, Z0107MN, Z0109MN

Sensitive Gate Triac Series

Silicon Bidirectional Thyristors

Designed for use in solid state relays, MPU interface, TTL logic and other light industrial or consumer applications. Supplied in surface mount package for use in automated manufacturing.

Features

- Sensitive Gate Trigger Current in Four Trigger Modes
- Blocking Voltage to 600 V
- Glass Passivated Surface for Reliability and Uniformity
- Surface Mount Package
- These are Pb-Free Devices

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (Note 1) (Sine Wave, 50 to 60 Hz, Gate Open, T _J = -40 to +125°C)	V _{DRM} , V _{RRM}	600	V
On-State Current RMS (T _C = 80°C) (Full Sine Wave 50 to 60 Hz)	I _{T(RMS)}	1.0	A
Peak Non-repetitive Surge Current (One Full Cycle Sine Wave, 60 Hz, T _C = 25°C)	I _{TSM}	8.0	A
Circuit Fusing Considerations (Pulse Width = 8.3 ms)	I ² t	0.4	A ² s
Average Gate Power (T _C = 80°C, t ≤ 8.3 ms)	P _{G(AV)}	1.0	W
Peak Gate Current (t ≤ 20 μs, T _J = +125°C)	I _{GM}	1.0	A
Operating Junction Temperature Range	T _J	-40 to +125	°C
Storage Temperature Range	T _{stg}	-40 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

THERMAL CHARACTERISTICS

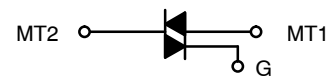
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Ambient PCB Mounted per Figure 1	R _{θJA}	156	°C/W
Thermal Resistance, Junction-to-Tab Meas- ured on MT2 Tab Adjacent to Epoxy	R _{θJT}	25	°C/W
Maximum Device Temperature for Soldering Purposes for 10 Secs Maximum	T _L	260	°C



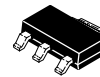
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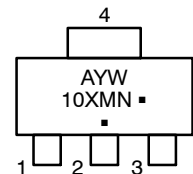
TRIAC 1.0 AMPERE RMS 600 VOLTS



MARKING DIAGRAM



SOT-223
CASE 318E
STYLE 11



A = Assembly Location
Y = Year
W = Work Week
10XMN = Device Code
x = 3, 7, 9
▪ = Pb-Free Package
(Note: Microdot may be in either location)

PIN ASSIGNMENT

Pin	Assignment
1	Main Terminal 1
2	Main Terminal 2
3	Gate
4	Main Terminal 2

ORDERING INFORMATION

Device	Package	Shipping†
Z0103MNT1G	SOT-223 (Pb-Free)	1000/Tape & Reel
Z0107MNT1G	SOT-223 (Pb-Free)	1000/Tape & Reel
Z0109MNT1G	SOT-223 (Pb-Free)	1000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted; Electricals apply in both directions)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Peak Repetitive Blocking Current ($V_D = \text{Rated } V_{DRM}$; V_{RRM} : Gate Open)	$T_J = 25^\circ\text{C}$ $T_J = +125^\circ\text{C}$	I_{DRM} , I_{RRM}	-	-	5.0 500	μA μA
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ON CHARACTERISTICS

Peak On-State Voltage ($I_{TM} = \pm 1.4 \text{ A Peak}$; Pulse Width $\leq 2.0 \text{ ms}$, Duty Cycle $\leq 2.0\%$)		V_{TM}	-	-	1.56	V
Gate Trigger Current (Continuous dc) ($V_D = 12 \text{ Vdc}$, $R_L = 30 \text{ Ohms}$) MT2(+), G(+) MT2(+), G(-) MT2(-), G(-) MT2(-), G(+)	Z0103MN	I_{GT}	0.15 0.15 0.15 0.25	- - - -	3.0 3.0 3.0 5.0	mA
Gate Trigger Current (Continuous dc) ($V_D = 12 \text{ Vdc}$, $R_L = 30 \text{ Ohms}$) MT2(+), G(+) MT2(+), G(-) MT2(-), G(-) MT2(-), G(+)	Z0107MN	I_{GT}	0.15 0.15 0.15 0.25	- - - -	5.0 5.0 5.0 7.0	mA
Gate Trigger Current (Continuous dc) ($V_D = 12 \text{ Vdc}$, $R_L = 30 \text{ Ohms}$) MT2(+), G(+) MT2(+), G(-) MT2(-), G(-) MT2(-), G(+)	Z0109MN	I_{GT}	0.15 0.15 0.15 0.25	- - - -	10 10 10 10	mA
Latching Current ($V_D = 12 \text{ V}$, $I_G = 1.2 \times I_{GT}$) MT2(+), G(+) MT2(+), G(-) MT2(-), G(-) MT2(-), G(+)	Z0103MN	I_L	- - - -	- - - -	7.0 15 7.0 7.0	mA
Latching Current ($V_D = 12 \text{ V}$, $I_G = 1.2 \times I_{GT}$) MT2(+), G(+) MT2(+), G(-) MT2(-), G(-) MT2(-), G(+)	Z0107MN	I_L	- - - -	- - - -	10 20 10 10	mA
Latching Current ($V_D = 12 \text{ V}$, $I_G = 1.2 \times I_{GT}$) MT2(+), G(+) MT2(+), G(-) MT2(-), G(-) MT2(-), G(+)	Z0109MN	I_L	- - - -	- - - -	15 25 15 15	mA
Gate Trigger Voltage (Continuous dc) ($V_D = 12 \text{ Vdc}$, $R_L = 30 \text{ Ohms}$)		V_{GT}	-	-	1.3	V
Gate Non-Trigger Voltage ($V_D = 12 \text{ V}$, $R_L = 30 \text{ Ohms}$, $T_J = 125^\circ\text{C}$) All Four Quadrants		V_{GD}	0.2	-	-	V
Holding Current ($V_D = 12 \text{ Vdc}$, Initiating Current = 50 mA, Gate Open)	(Z0103MA) (Z0107MA, Z0109MA)	I_H	- -	- -	7.0 10	mA

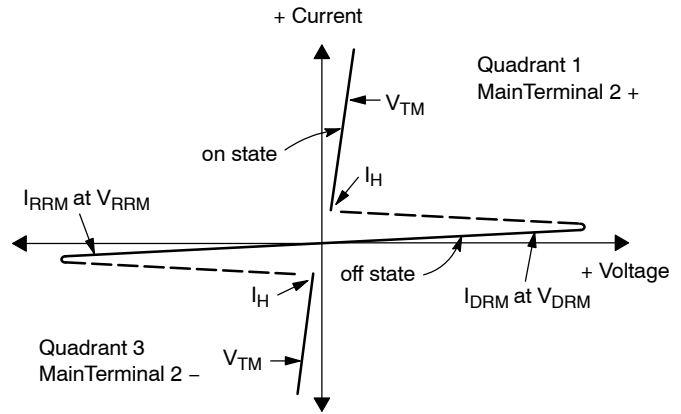
DYNAMIC CHARACTERISTICS

Rate of Change of Commutating Current ($V_D = 400 \text{ V}$, $I_{TM} = 0.84 \text{ A}$, Commutating $dv/dt = 1.5 \text{ V}/\mu\text{s}$, Gate Open, $T_J = 110^\circ\text{C}$, $f = 250 \text{ Hz}$, with Snubber)		$di/dt(c)$	1.6	-	-	A/ms
Critical Rate of Rise of Off-State Voltage ($V_D = 67\%$ Rated V_{DRM} , Exponential Waveform, Gate Open, $T_J = 110^\circ\text{C}$)	Z0103MN Z0107MN Z0109MN	dv/dt	10 20 50	30 60 75	- - -	V/ μs
Repetitive Critical Rate of Rise of On-State Current, $T_J = 125^\circ\text{C}$ Pulse Width = 20 μs , $I_{PKmax} = 15 \text{ A}$, $di/dt = 1 \text{ A}/\mu\text{s}$, $f = 60 \text{ Hz}$		di/dt	-	-	20	A/ μs

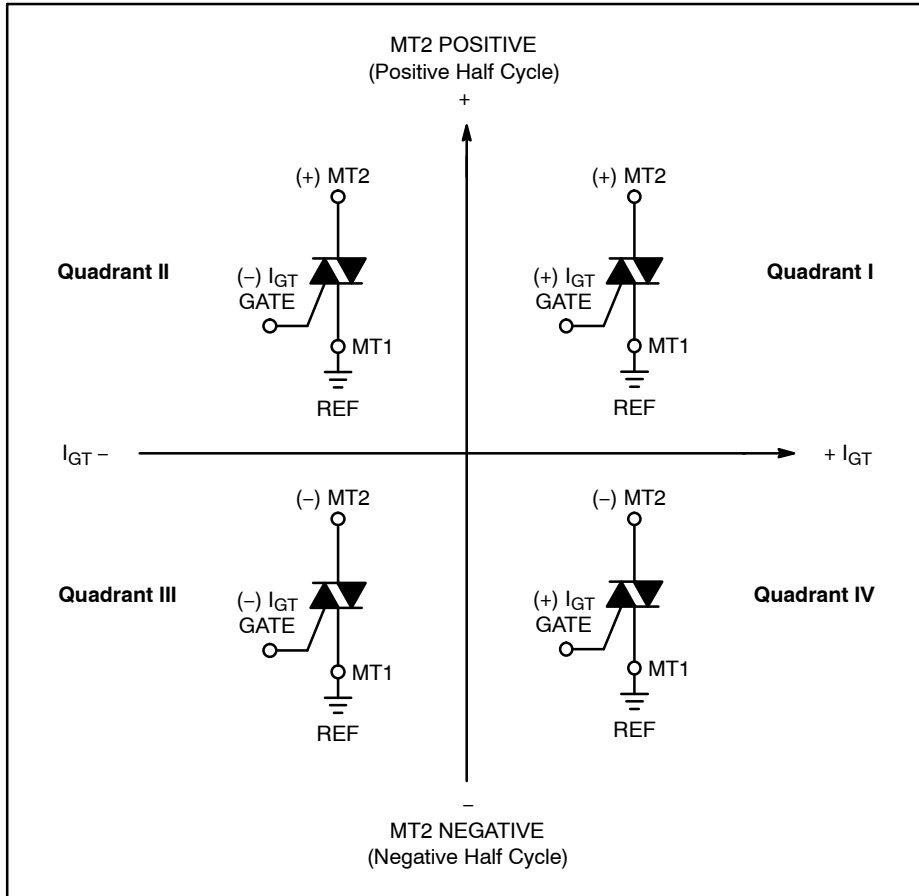
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Voltage Current Characteristic of Triacs (Bidirectional Device)

Symbol	Parameter
V_{DRM}	Peak Repetitive Forward Off State Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Reverse Off State Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Maximum On State Voltage
I_H	Holding Current

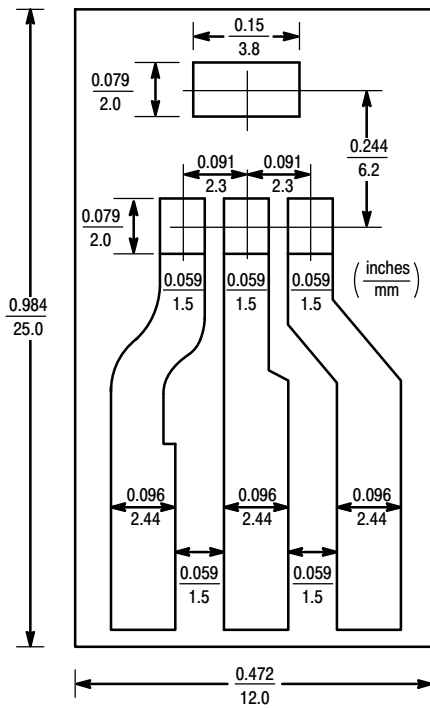


Quadrant Definitions for a Triac



All polarities are referenced to MT1.
With in-phase signals (using standard AC lines) quadrants I and III are used.

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BOARD MOUNTED VERTICALLY IN CINCH 8840 EDGE CONNECTOR.
 BOARD THICKNESS = 65 MIL, FOIL THICKNESS = 2.5 MIL
 MATERIAL: G10 FIBERGLASS BASE EPOXY

Figure 1. PCB for Thermal Impedance and Power Testing of SOT-223

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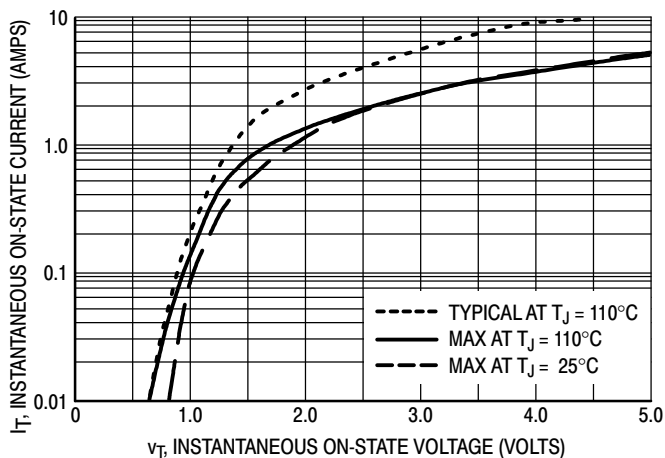


Figure 2. On-State Characteristics

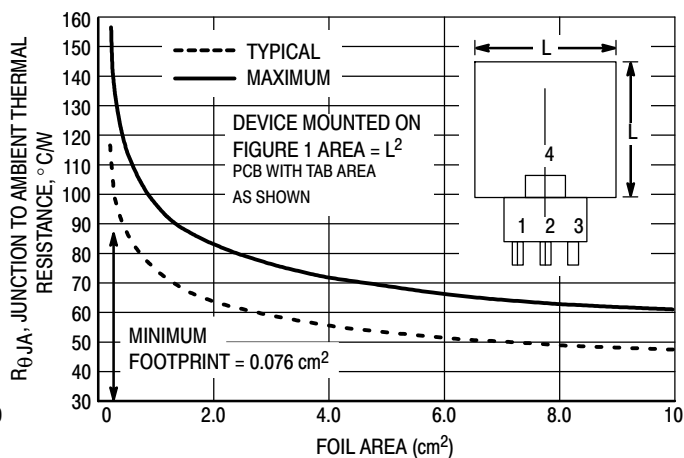


Figure 3. Junction to Ambient Thermal Resistance versus Copper Tab Area

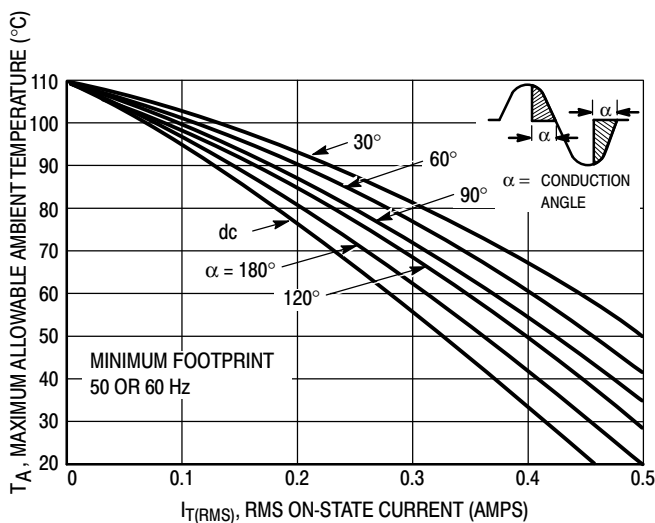


Figure 4. Current Derating, Minimum Pad Size Reference: Ambient Temperature

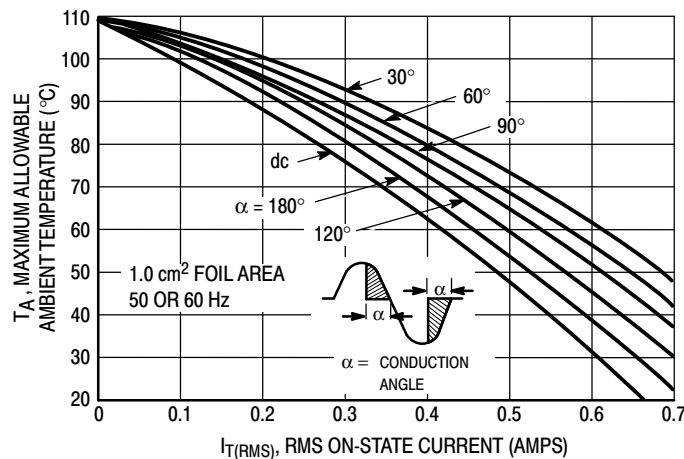


Figure 5. Current Derating, 1.0 cm Square Pad Reference: Ambient Temperature

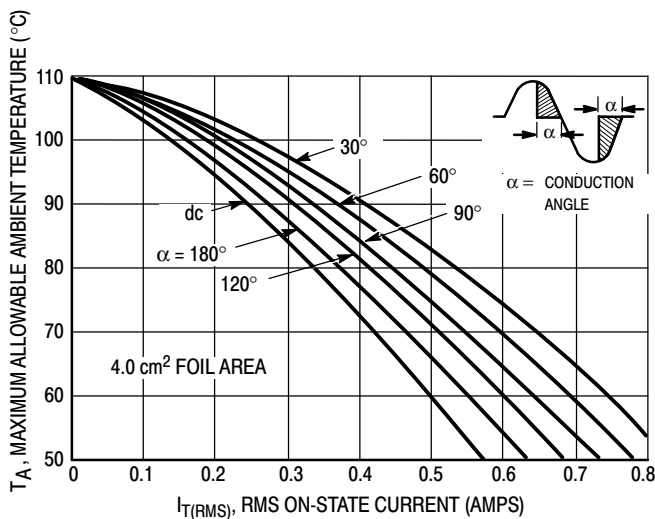


Figure 6. Current Derating, 2.0 cm Square Pad Reference: Ambient Temperature

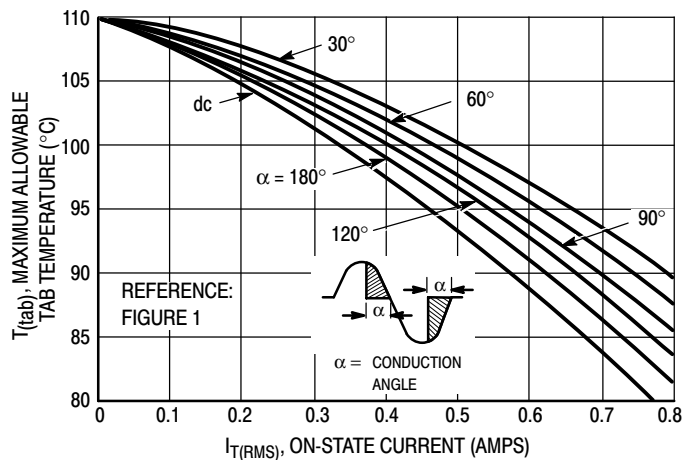


Figure 7. Current Derating Reference: MT2 Tab

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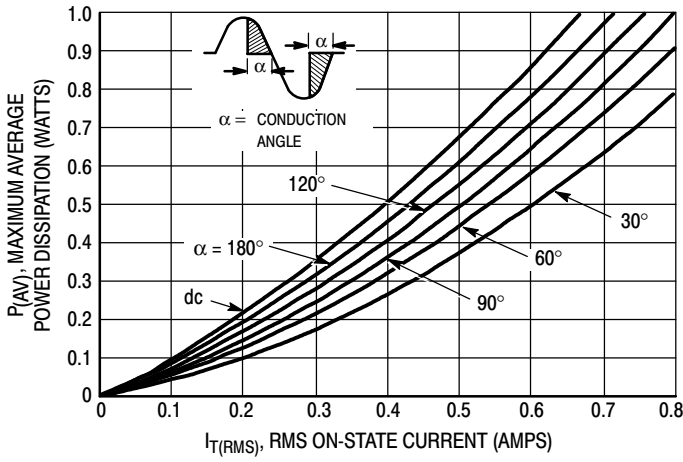


Figure 8. Power Dissipation

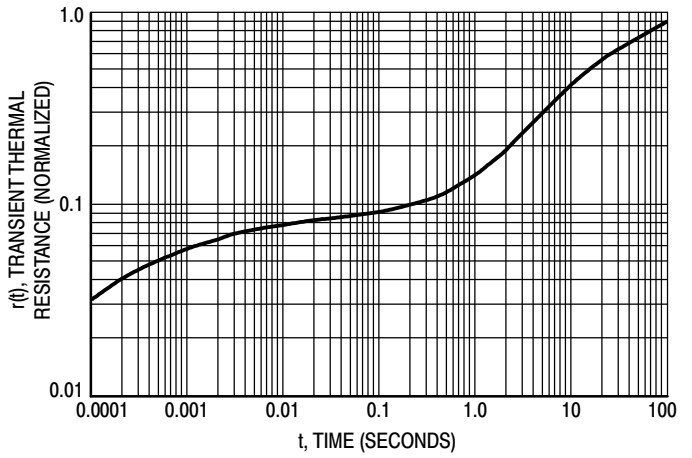
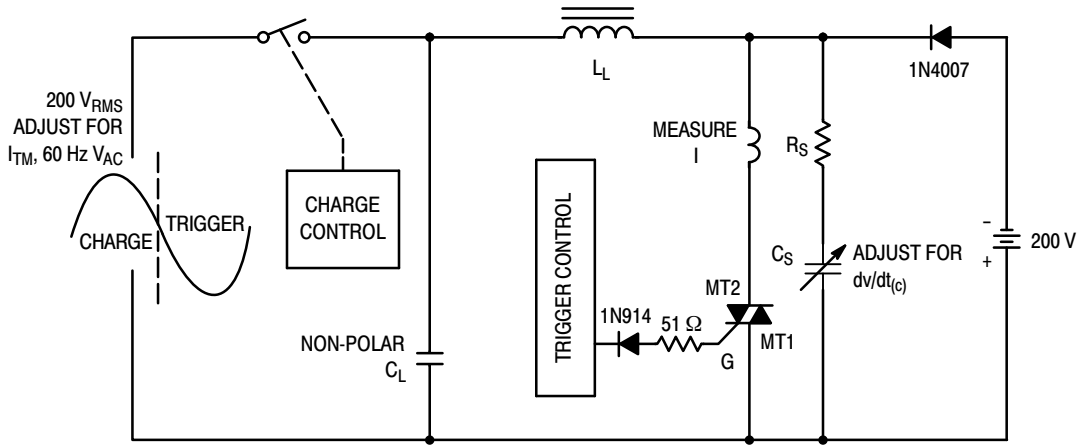


Figure 9. Thermal Response, Device Mounted on Figure 1 Printed Circuit Board



Note: Component values are for verification of rated (dv/dt)_c. See AN1048 for additional information.

Figure 10. Simplified Test Circuit to Measure the Critical Rate of Rise of Commutating Voltage (dv/dt)_c

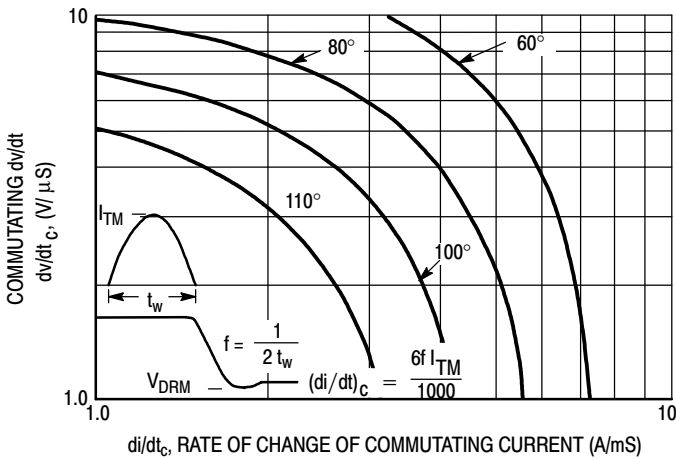


Figure 11. Typical Commutating dv/dt versus Current Crossing Rate and Junction Temperature

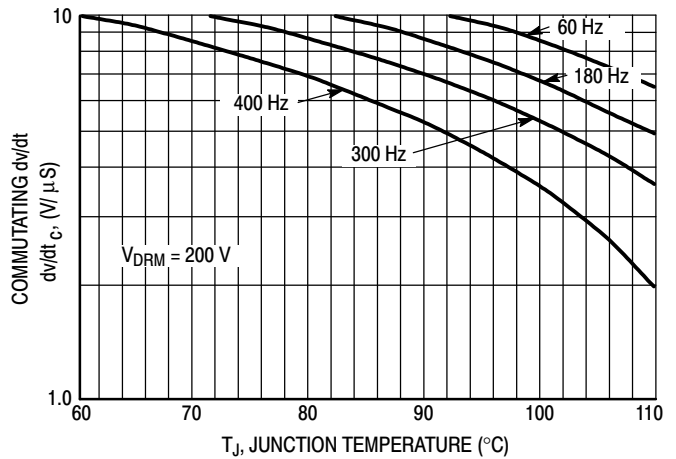


Figure 12. Typical Commutating dv/dt versus Junction Temperature at 0.8 Amps RMS

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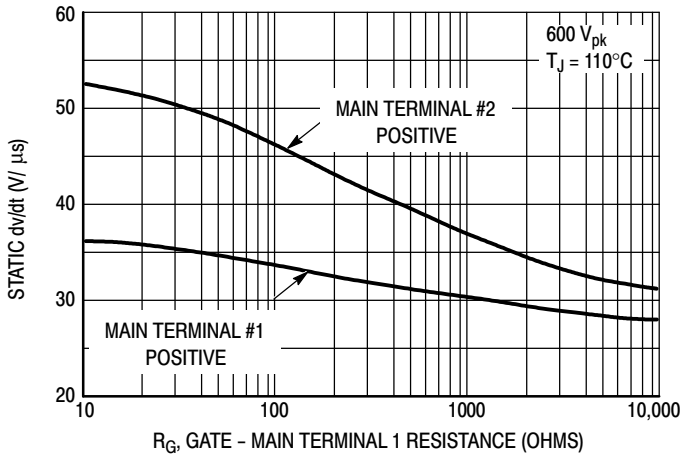


Figure 13. Exponential Static dv/dt versus Gate - Main Terminal 1 Resistance

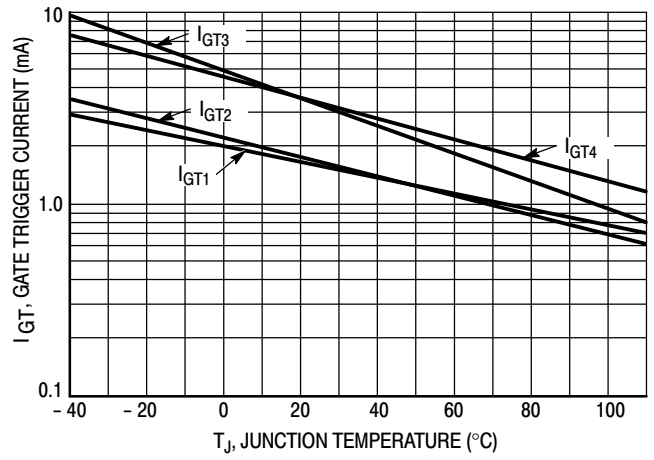


Figure 14. Typical Gate Trigger Current Variation

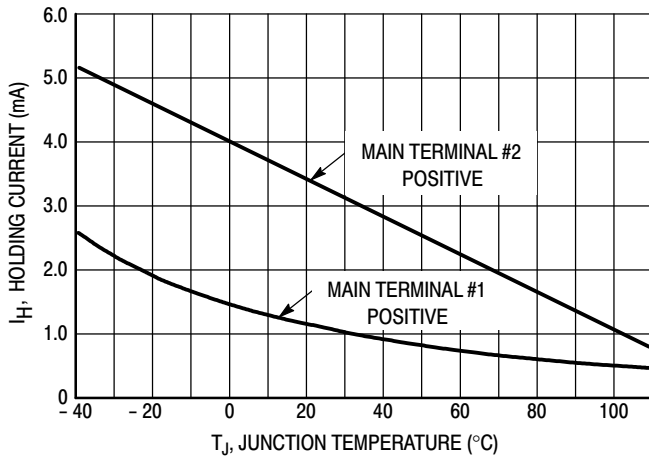


Figure 15. Typical Holding Current Variation

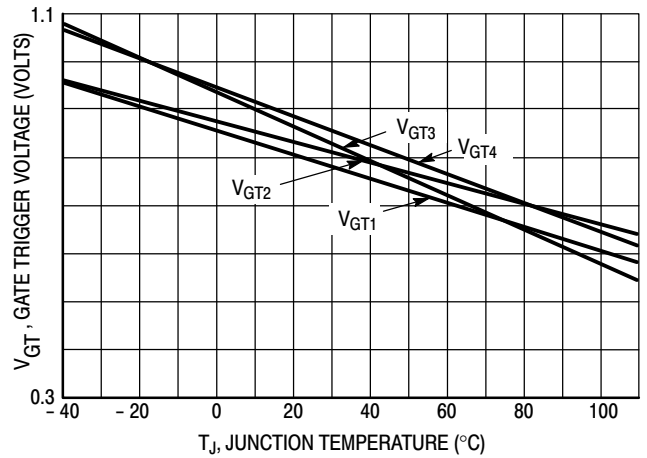
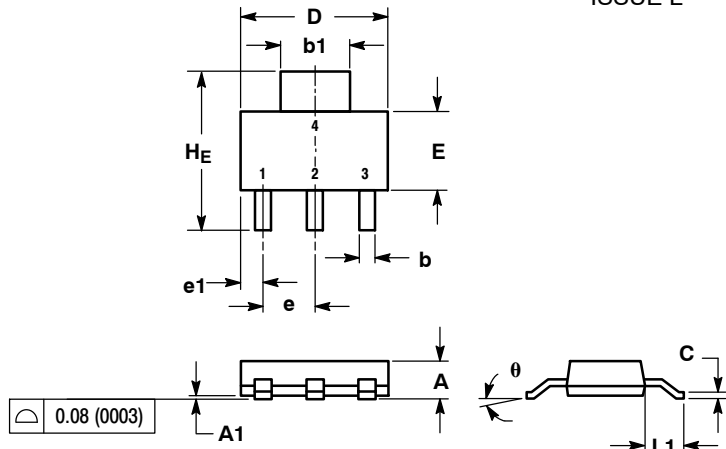


Figure 16. Gate Trigger Voltage Variation

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PACKAGE DIMENSIONS

SOT-223 (TO-261)
CASE 318E-04
ISSUE L

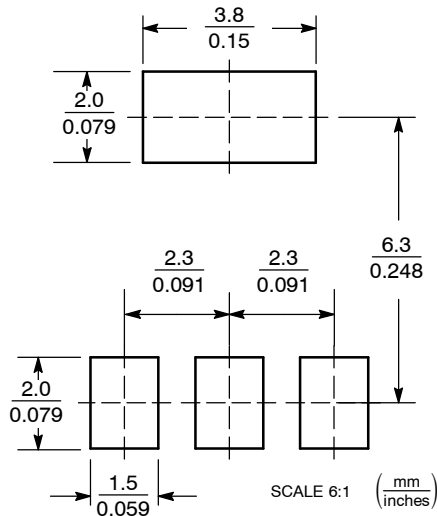


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.63	1.75	0.060	0.064	0.068
A1	0.02	0.06	0.10	0.001	0.002	0.004
b	0.60	0.75	0.89	0.024	0.030	0.035
b1	2.90	3.06	3.20	0.115	0.121	0.126
c	0.24	0.29	0.35	0.009	0.012	0.014
D	6.30	6.50	6.70	0.249	0.256	0.263
E	3.30	3.50	3.70	0.130	0.138	0.145
e	2.20	2.30	2.40	0.087	0.091	0.094
e1	0.85	0.94	1.05	0.033	0.037	0.041
L1	1.50	1.75	2.00	0.060	0.069	0.078
HE	6.70	7.00	7.30	0.264	0.276	0.287
θ	0°	-	10°	0°	-	10°

STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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