# **EFC4618R-P**



# Power MOSFET 24V, 6A, 23mΩ, Dual N-Channel

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#### **Features**

- · 2.5V Drive
- · Best Suited for LiB Charging and Discharging Switch
- · Common-drain Type
- · ESD Diode Protected Gate
- · Pb-Free, Halogen Free and RoHS Compliance

# **Specifications**

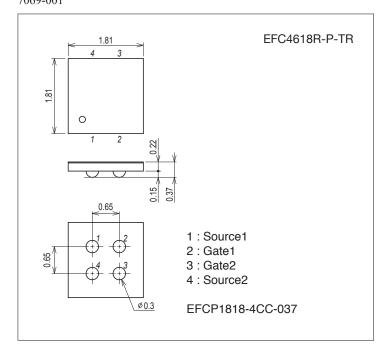
# Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Source-to-Source Voltage	VSSS		24	V
Gate-to-Source Voltage	VGSS		±12	V
Source Current (DC)	Is		6	Α
Source Current (Pulse)	ISP	PW≤10μs, duty cycle≤1%	60	Α
Total Dissipation	PT	When mounted on ceramic substrate (5000mm <sup>2</sup> ×0.8mm)	1.6	W
Channel Temperature	Tch		150	°C
Storage Temperature	Tstg		-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### **Package Dimensions**

unit : mm (typ) 7069-001



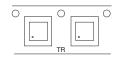
#### **Product & Package Information**

• Package : EFCP

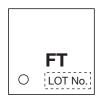
• JEITA, JEDEC :-

• Minimum Packing Quantity : 5,000 pcs./reel

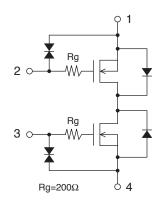
## Packing Type: TR



## Marking



#### **Electrical Connection**



# **ORDERING INFORMATION**

See detailed ordering and shipping information on page 2 of this data sheet.

# **EFC4618R-P**

#### **Electrical Characteristics** at Ta=25°C

Parameter	0	Conditions		Ratings			1.1-24
Parameter	Symbol			min	typ	max	Unit
Source-to-Source Breakdown Voltage	V(BR)SSS	I <sub>S</sub> =1mA, V <sub>GS</sub> =0V	Test Circuit 1	24			V
Zero-Gate Voltage Source Current	Isss	VSS=20V, VGS=0V	Test Circuit 1			1	μΑ
Gate-to-Source Leakage Current	IGSS	VGS=±8V, VSS=0V	Test Circuit 2			±10	μΑ
Cutoff Voltage	V <sub>GS</sub> (off)	V <sub>SS</sub> =10V, I <sub>S</sub> =1mA	Test Circuit 3	0.5		1.3	V
Forward Transfer Admittance	yfs	V <sub>SS</sub> =10V, I <sub>S</sub> =3A	Test Circuit 4		6.5		S
Static Source-to-Source On-State Resistance	Rss(on)1	IS=3A, VGS=4.5V	Test Circuit 5	13.5	19.8	23	mΩ
	Rss(on)2	I <sub>S</sub> =3A, V <sub>GS</sub> =4.0V	Test Circuit 5	14	20.5	24	mΩ
	R <sub>SS</sub> (on)3	I <sub>S</sub> =3A, V <sub>GS</sub> =3.7V	Test Circuit 5	14.5	21	25.5	mΩ
	Rss(on)4	I <sub>S</sub> =3A, V <sub>GS</sub> =3.1V	Test Circuit 5	14.9	23	30	mΩ
	Rss(on)5	IS=3A, VGS=2.5V	Test Circuit 5	18.5	27	35	mΩ
Turn-ON Delay Time	t <sub>d</sub> (on)		Test Circuit 7		200		ns
Rise Time	t <sub>r</sub>	Con an acified Test Circuit			815		ns
Turn-OFF Delay Time	t <sub>d</sub> (off)	See specified Test Circuit.			1840		ns
Fall Time	tf	]			1770		ns
Total Gate Charge	Qg	V <sub>SS</sub> =10V, V <sub>GS</sub> =4.5V, I <sub>S</sub> =6A			25.4		nC
Forward Source-to-Source Voltage	VF(S-S)	I <sub>S</sub> =3A, V <sub>GS</sub> =0V Test Circuit 6			0.76	1.2	V

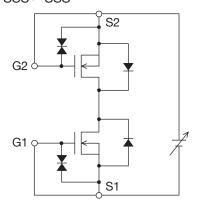
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

#### **ORDERING INFORMATION**

Device	Package	Shipping	memo	
EFC4618R-P-TR EFCP		5,000pcs./reel	Pb-Free and Halogen Free	

# Test circuits are example of measuring FET1 side

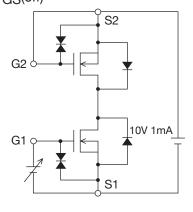
Test Circuit 1 VSSS / ISSS



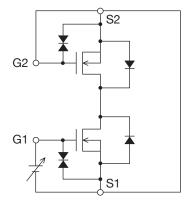
IT11565

IT11567

Test Circuit 3 VGS(off)



Test Circuit 2 IGSS(+) / (-)



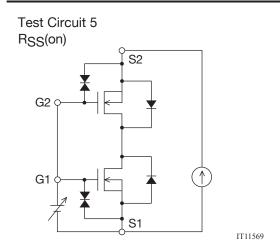
IT11566

IT11568

Test Circuit 4

G1 S1 S1

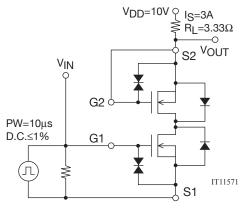
\* Note: Connect the mesurement terminal reversely if you want to measure the FET2 side.

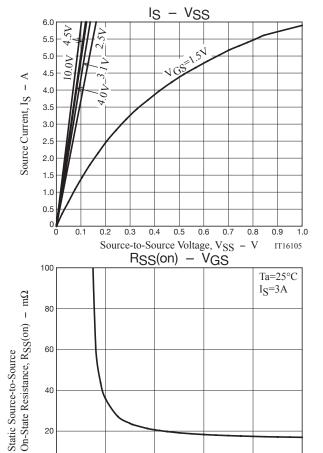


Test Circuit 7  $t_d(on)$ ,  $t_r$ ,  $t_d(off)$ ,  $t_f$ 

20

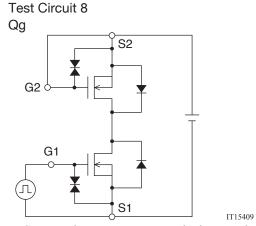
0



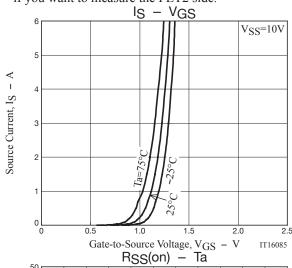


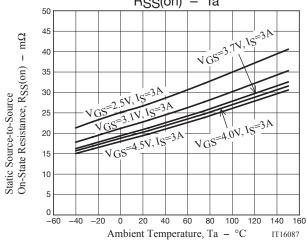
Gate-to-Source Voltage,  $V_{GS} - V$ 

# Test Circuit 6 VF(S-S) S2 4.5V G2 G1 S1 IT11570

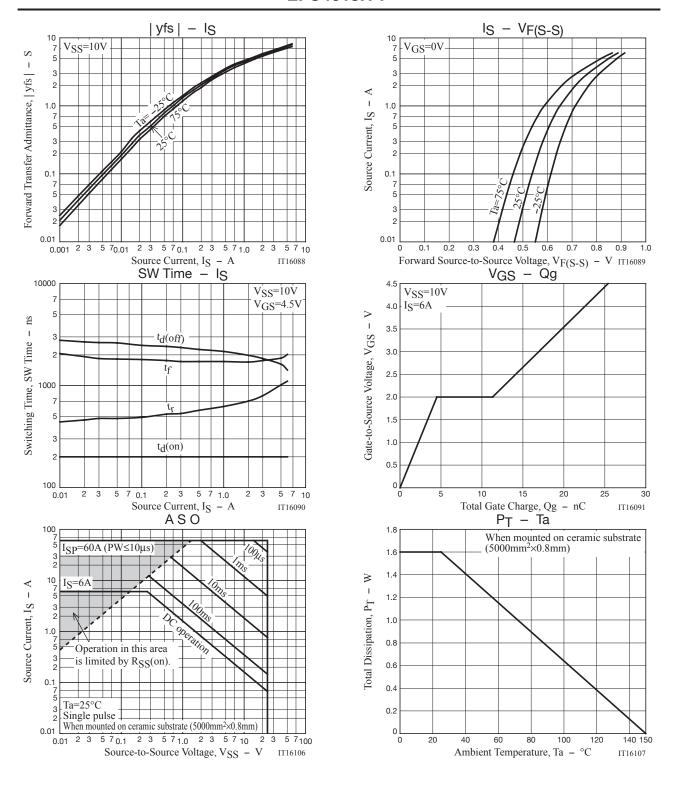


\* Note: Connect the mesurement terminal reversely if you want to measure the FET2 side.





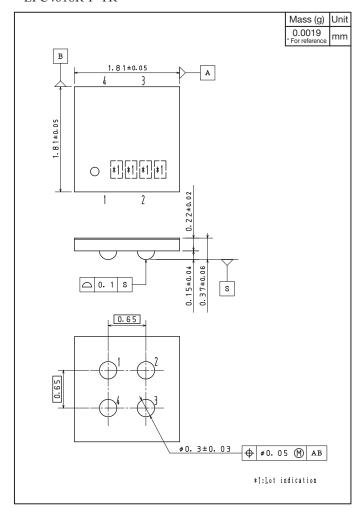
IT16086

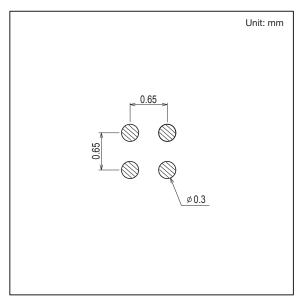


#### **Outline Drawing**

EFC4618R-P-TR

#### **Land Pattern Example**





Note on usage: Since the EFC4618R-P is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

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