

PSMN023-40YLC

N-channel 40 V 23mΩ logic level MOSFET in LFPACK using NextPower technology

22 August 2012

Product data sheet

1. Product profile

1.1 General description

Logic level enhancement mode N-channel MOSFET in LFPACK package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High reliability Power SO8 package, qualified to 175°C
- Low parasitic inductance
- Optimised for 4.5V Gate drive utilising NextPower Superjunction technology
- Ultra low QG, QGD, & QOSS for high system efficiencies at low and high loads

1.3 Applications

- DC-to-DC converters
- Load switching
- Server power supplies
- Synchronous buck regulator

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C	-	-	40	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; Fig. 1	-	-	24	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 2	-	-	25	W
T _j	junction temperature		-55	-	175	°C
Static characteristics						
R _{DSon}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 5 A; T _j = 25 °C; Fig. 12	-	22	26	mΩ
		V _{GS} = 10 V; I _D = 5 A; T _j = 25 °C; Fig. 12	-	19	23	mΩ
Dynamic characteristics						
Q _{GD}	gate-drain charge	V _{GS} = 4.5 V; I _D = 5 A; V _{DS} = 20 V; Fig. 14 ; Fig. 15	-	0.9	-	nC

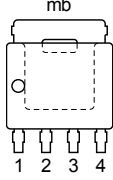
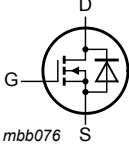


N-channel 40 V 23mΩ logic level MOSFET in LPAK using NextPower technology

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Q_{G(tot)}$	total gate charge	$V_{GS} = 4.5\text{ V}$; $I_D = 5\text{ A}$; $V_{DS} = 20\text{ V}$; Fig. 14 ; Fig. 15	-	4.3	-	nC

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LPAK; Power-SO8 (SOT669)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN023-40YLC	LPAK; Power-SO8	plastic single-ended surface-mounted package; 4 leads	SOT669

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	40	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	40	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 1	-	24	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 1	-	17	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 4	-	97	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 2	-	25	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
V_{ESD}	electrostatic discharge voltage	MM (JEDEC JESD22-A115)	100	-	V

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Symbol	Parameter	Conditions	Min	Max	Unit
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ }^\circ\text{C}$	-	23	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ }^\circ\text{C}$	-	97	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; $I_D = 24\text{ A}$; $V_{sup} \leq 40\text{ V}$; $R_{GS} = 50\text{ }\Omega$; unclamped; Fig. 3	-	6.9	mJ

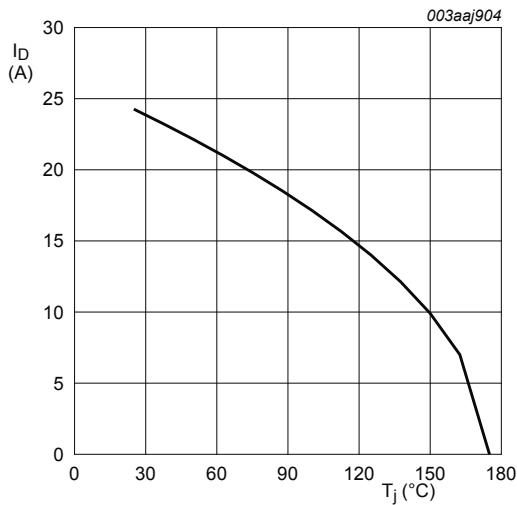


Fig. 1. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 10V$$

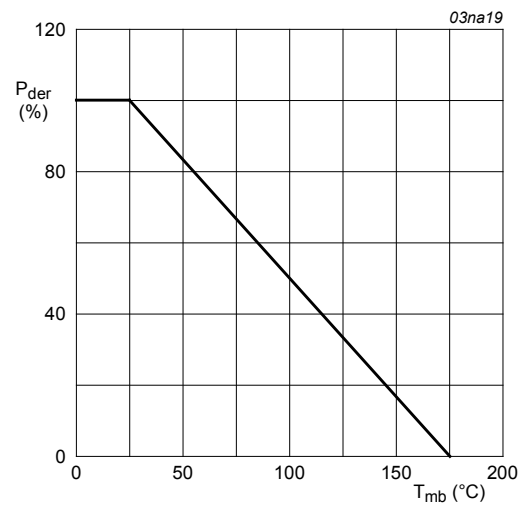


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

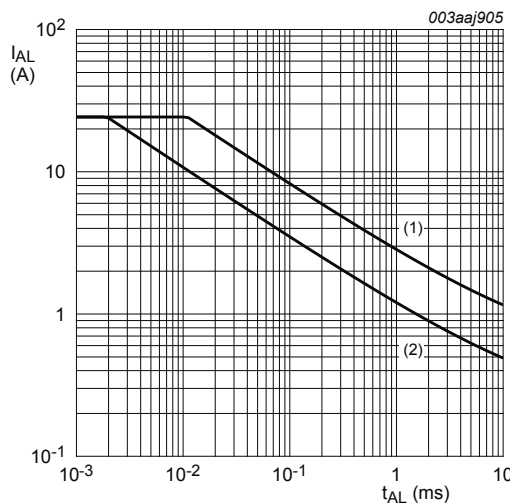


Fig. 3. Single pulse avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; (2) $T_{j(\text{init})} = 100\text{ }^\circ\text{C}$

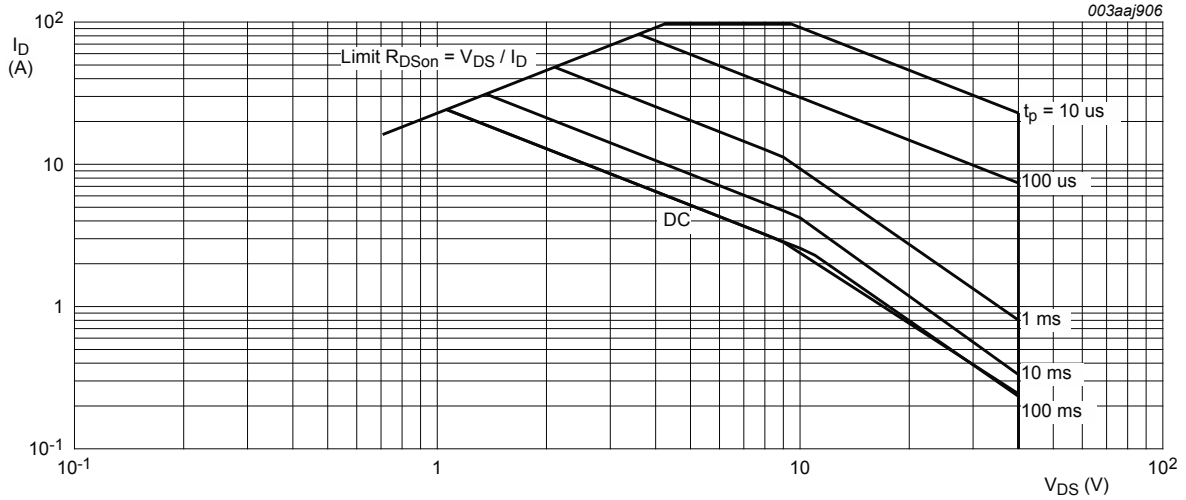


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^\circ C$; I_{DM} is a single pulse

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	5.66	5.83	K/W

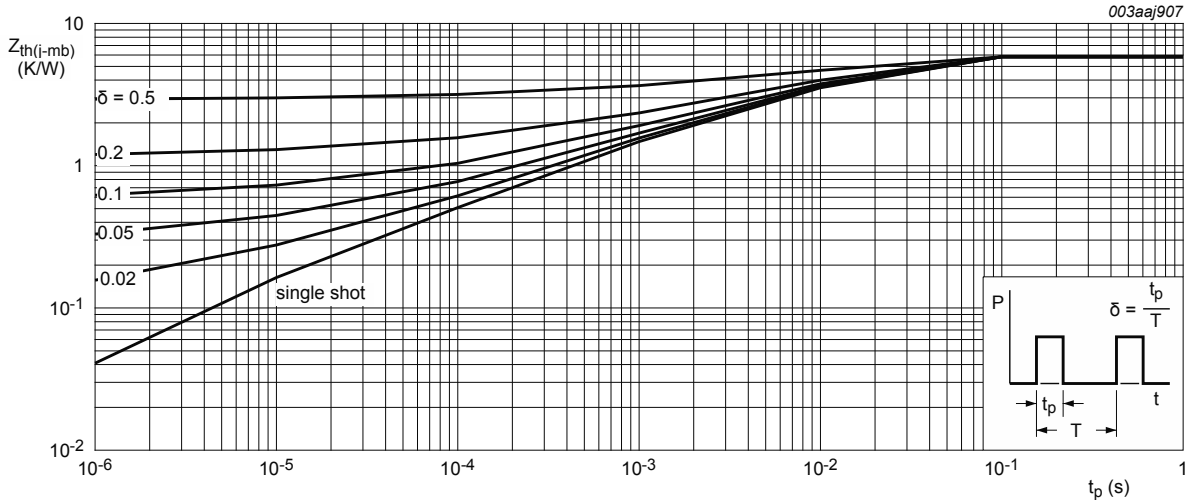


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	40	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ Fig. 10	1.05	1.67	1.95	V
		$I_D = 10 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ C;$ Fig. 11	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ Fig. 11	-	-	2.25	V
I_{DSS}	drain leakage current	$V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	1	μA
		$V_{DS} = 40 V; V_{GS} = 0 V; T_j = 150 \text{ }^\circ C$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5 V; I_D = 5 A; T_j = 25 \text{ }^\circ C;$ Fig. 12	-	22	26	mΩ
		$V_{GS} = 4.5 V; I_D = 5 A; T_j = 150 \text{ }^\circ C;$ Fig. 12; Fig. 13	-	-	44.5	mΩ
		$V_{GS} = 10 V; I_D = 5 A; T_j = 25 \text{ }^\circ C;$ Fig. 12	-	19	23	mΩ
		$V_{GS} = 10 V; I_D = 5 A; T_j = 150 \text{ }^\circ C;$ Fig. 12; Fig. 13	-	-	39.5	mΩ
R_G	gate resistance	$f = 1 \text{ MHz}$	0.85	1.7	3.4	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 5 A; V_{DS} = 20 V; V_{GS} = 10 V;$ Fig. 14; Fig. 15	-	8.4	-	nC
		$I_D = 5 A; V_{DS} = 20 V; V_{GS} = 4.5 V;$ Fig. 14; Fig. 15	-	4.3	-	nC
		$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$	-	8	-	nC
Q_{GS}	gate-source charge	$I_D = 5 A; V_{DS} = 20 V; V_{GS} = 4.5 V;$ Fig. 14; Fig. 15	-	1.3	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	0.7	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	0.6	-	nC
Q_{GD}	gate-drain charge		-	0.9	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 5 A; V_{DS} = 20 V;$ Fig. 14; Fig. 15	-	2.5	-	V

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{iss}	input capacitance	$V_{DS} = 20\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz};$	-	520	-	pF
C_{oss}	output capacitance	$T_j = 25\text{ }^\circ\text{C};$ Fig. 16	-	110	-	pF
C_{rss}	reverse transfer capacitance		-	40	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 20\text{ V}; R_L = 4\text{ } \Omega; V_{GS} = 4.5\text{ V};$	-	6.2	-	ns
t_r	rise time	$R_{G(ext)} = 5\text{ } \Omega$	-	3.8	-	ns
$t_{d(off)}$	turn-off delay time		-	9.9	-	ns
t_f	fall time		-	3.1	-	ns
Q_{oss}	output charge	$V_{GS} = 0\text{ V}; V_{DS} = 20\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^\circ\text{C}$	-	3.4	-	nC
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 5\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 17	-	0.83	1.1	V
t_{rr}	reverse recovery time	$I_S = 5\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$	-	12.9	-	ns
Q_r	recovered charge	$V_{DS} = 20\text{ V}$	-	6.9	-	nC
t_a	reverse recovery rise time	$V_{GS} = 0\text{ V}; I_S = 5\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s};$ $V_{DS} = 20\text{ V};$ Fig. 18	-	8.7	-	ns
t_b	reverse recovery fall time		-	4.2	-	ns

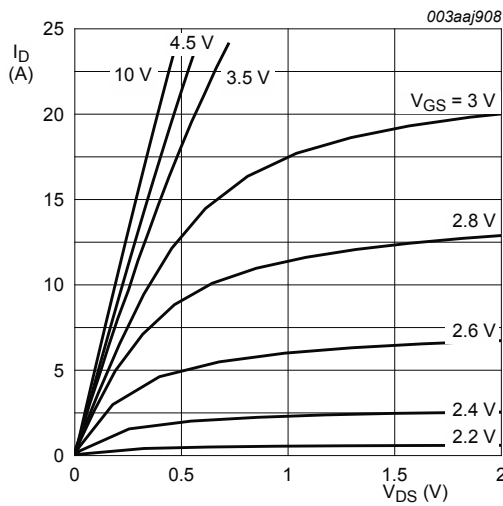


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

$T_j = 25^\circ\text{C}$

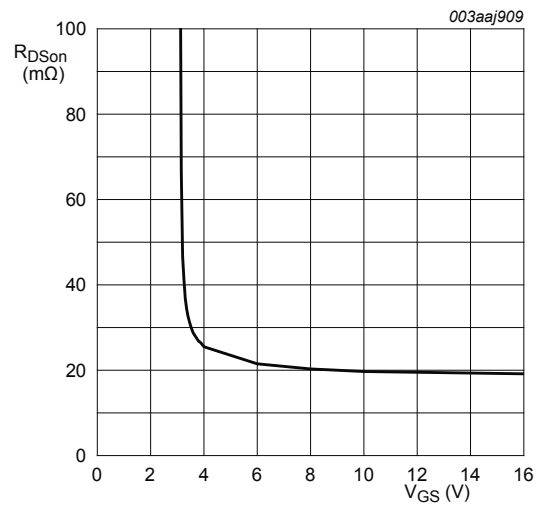


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25^\circ\text{C}; I_D = 5\text{ A}$

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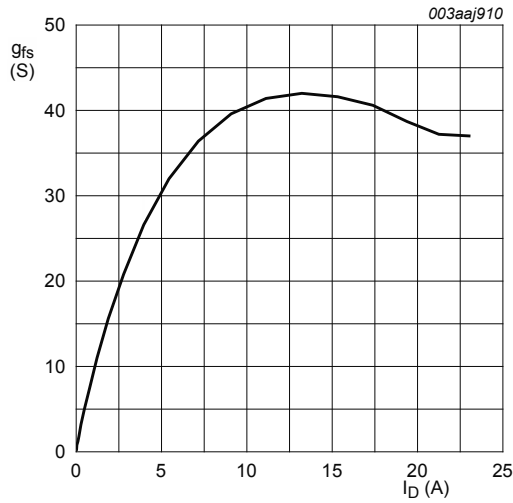


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_j = 25^\circ\text{C}; V_{DS} = 10\text{V}$

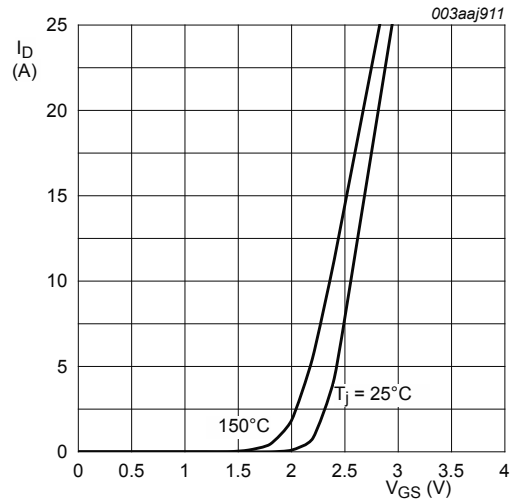


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10\text{V}$

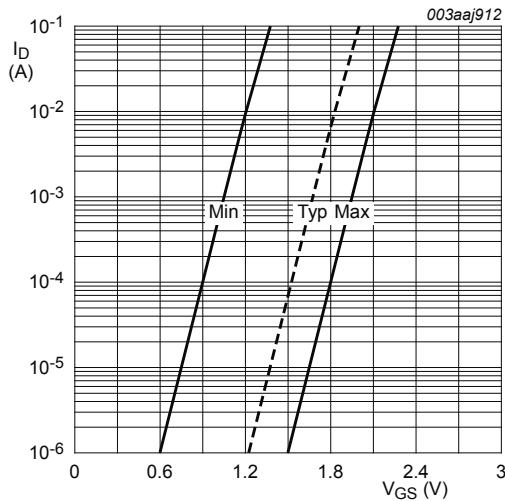


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$

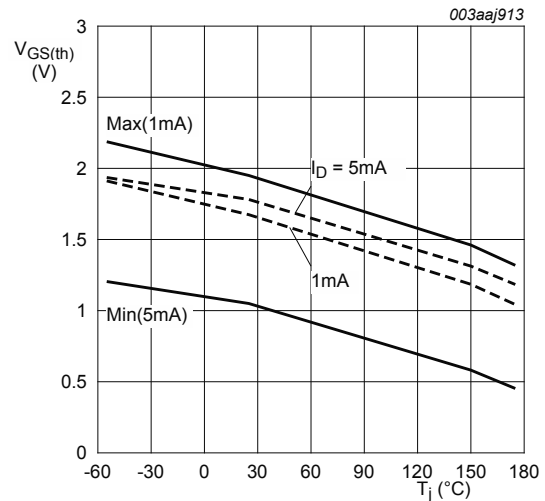


Fig. 11. Gate-source threshold voltage as a function of junction temperature

$V_{DS} = V_{GS}$

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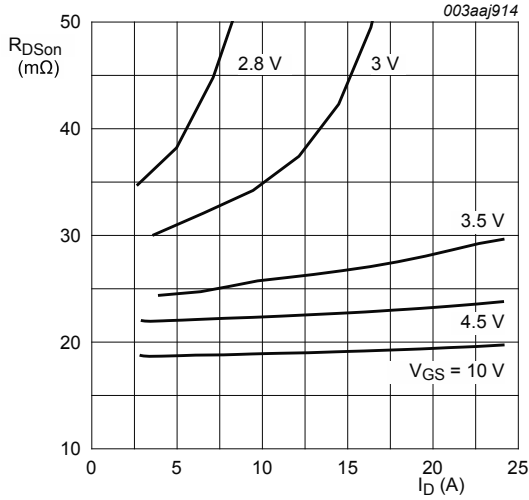


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25^\circ C$$

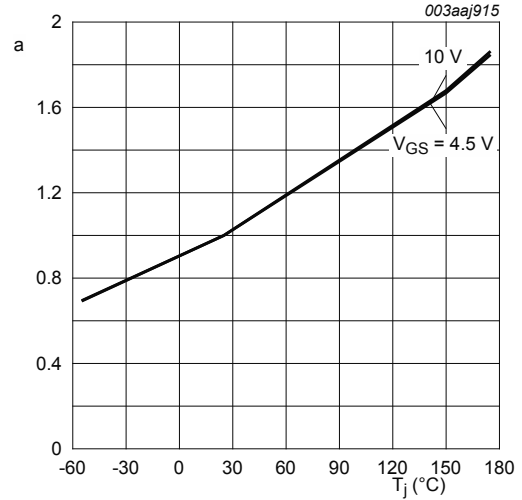


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)}(25^\circ C)}$$

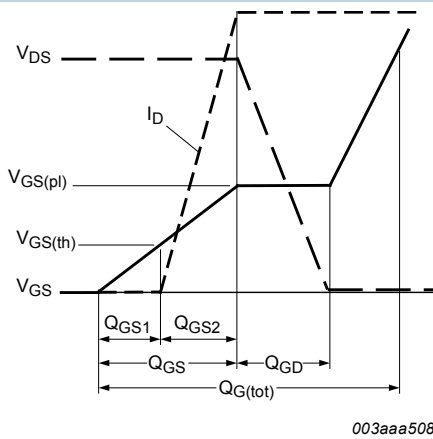


Fig. 14. Gate charge waveform definitions

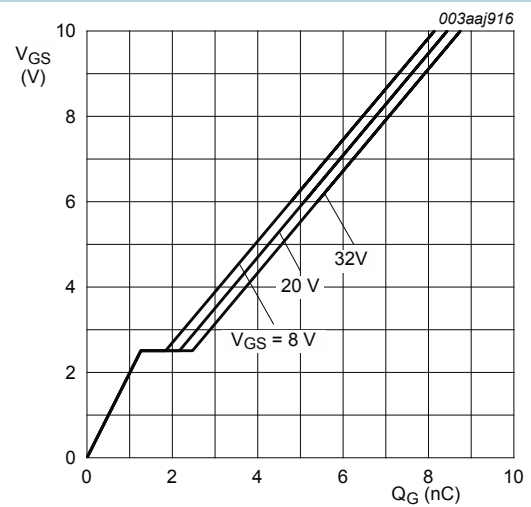


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25^\circ C; I_D = 5 A$$

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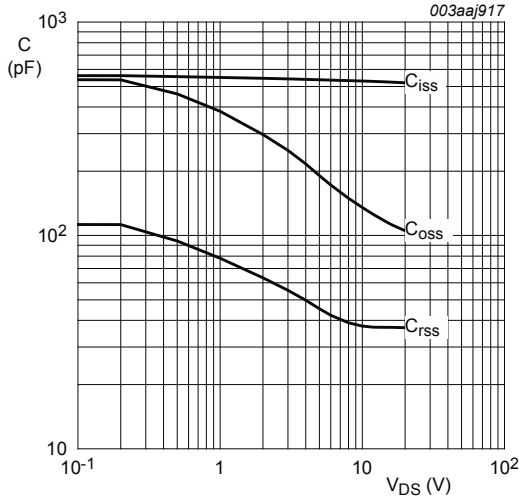


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0V; f = 1MHz$

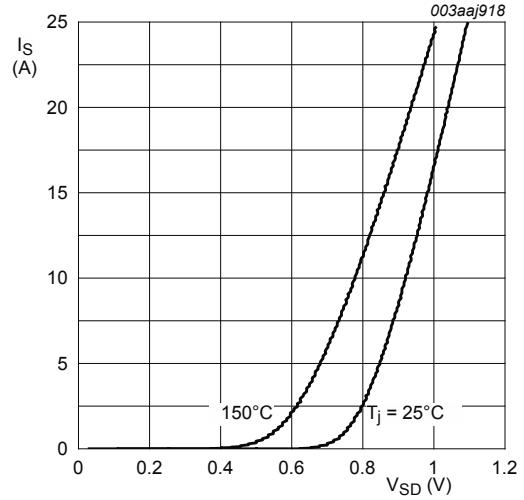


Fig. 17. Source current as a function of source-drain voltage; typical values

$V_{GS} = 0V$

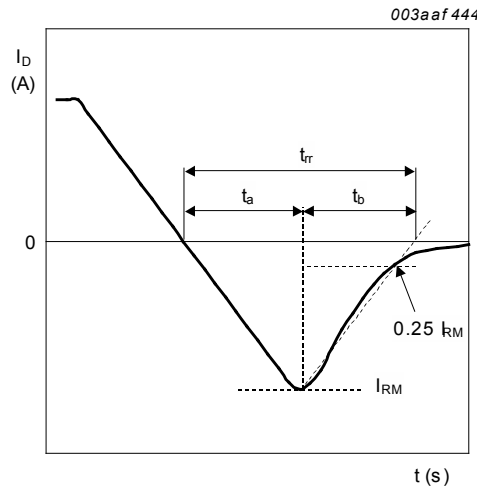


Fig. 18. Reverse recovery timing definition

7. Package outline

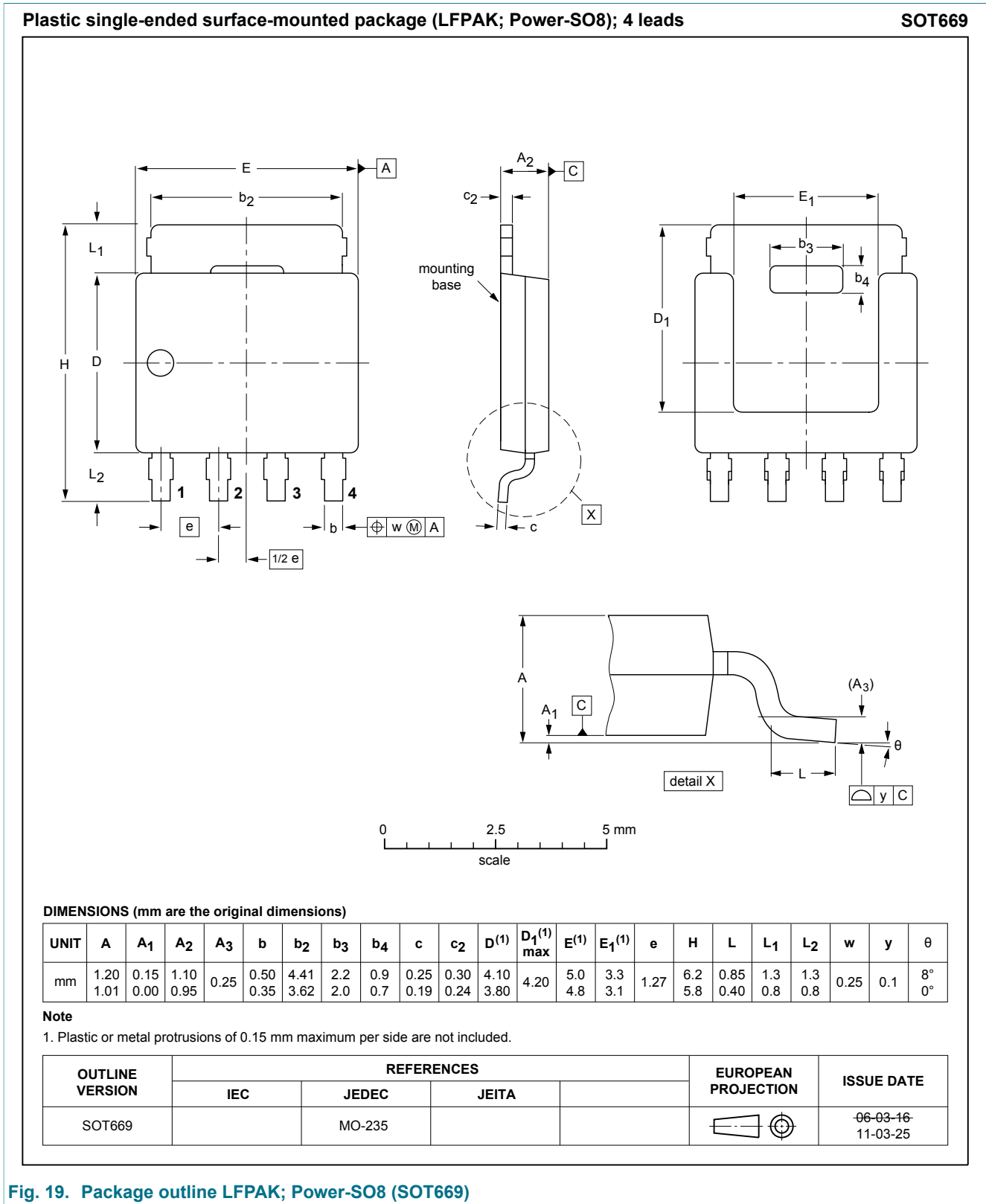


Fig. 19. Package outline LPAK; Power-SO8 (SOT669)

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8.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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