NCP439

2A Very Low Ron Switches at Low Vin Voltage

The NCP439 is a very low Ron MOSFET controlled by external logic pin, allowing optimization of battery life, and portable device autonomy.

This load switch is a best in class in term of $R_{DS(on)}$ optimization at low V_{IN} voltage.

Due to a current consumption optimization with PMOS structure, leakage currents are eliminated by isolating connected IC's on the battery when not used.

Output discharge path is also embedded to eliminate residual voltages on the output.

Proposed in wide input voltage range from 1.0 V to 3.6 V, and a very small 0.96 x 0.96 mm WLCSP4, 0.5 mm pitch.

Features

- 1 V – 3.6 V Operating Range
- 37 mΩ P MOSFET at 1.8 V
- DC Current Up to 2 A
- Output Auto−Discharge
- Active High EN Pin
- WLCSP4 0.96 x 0.96 mm
- This is a Pb−Free Device

Typical Applications

- Mobile Phones
- Tablets
- Digital Cameras
- GPS
- Portable Devices

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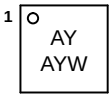
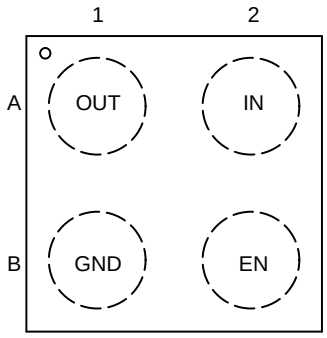
MARKING DIAGRAM

WLCSP4
CASE 567FG



AY	= Specific Device Code
A	= Assembly Location
Y	= Year
W	= Wafer Lot

PIN DIAGRAM



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

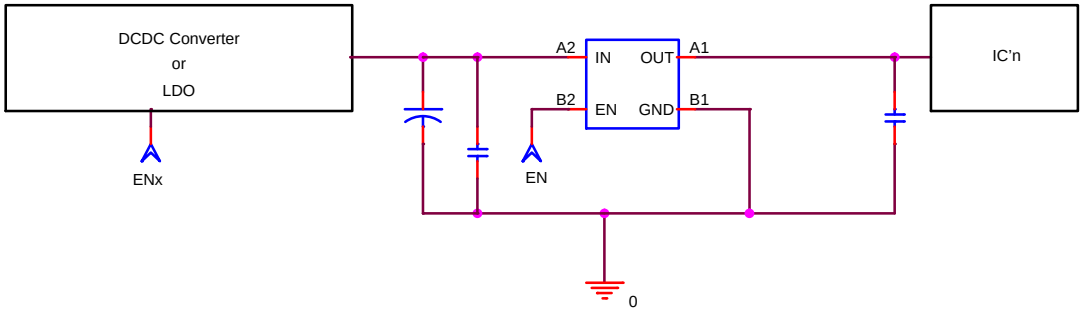


Figure 1. Typical Application Circuit

PIN FUNCTION DESCRIPTION

Pin Name	Pin Number	Type	Description
IN	A2	POWER	Load−switch input voltage; connect a 0.1 μF or greater ceramic capacitor from IN to GND as close as possible to the IC.
GND	B1	POWER	Ground connection.
EN	B2	INPUT	Enable input, logic high turns on power switch.
OUT	A1	OUTPUT	Load−switch output; connect a 0.1 μF ceramic capacitor from OUT to GND as close as possible to the IC is recommended.

BLOCK DIAGRAM

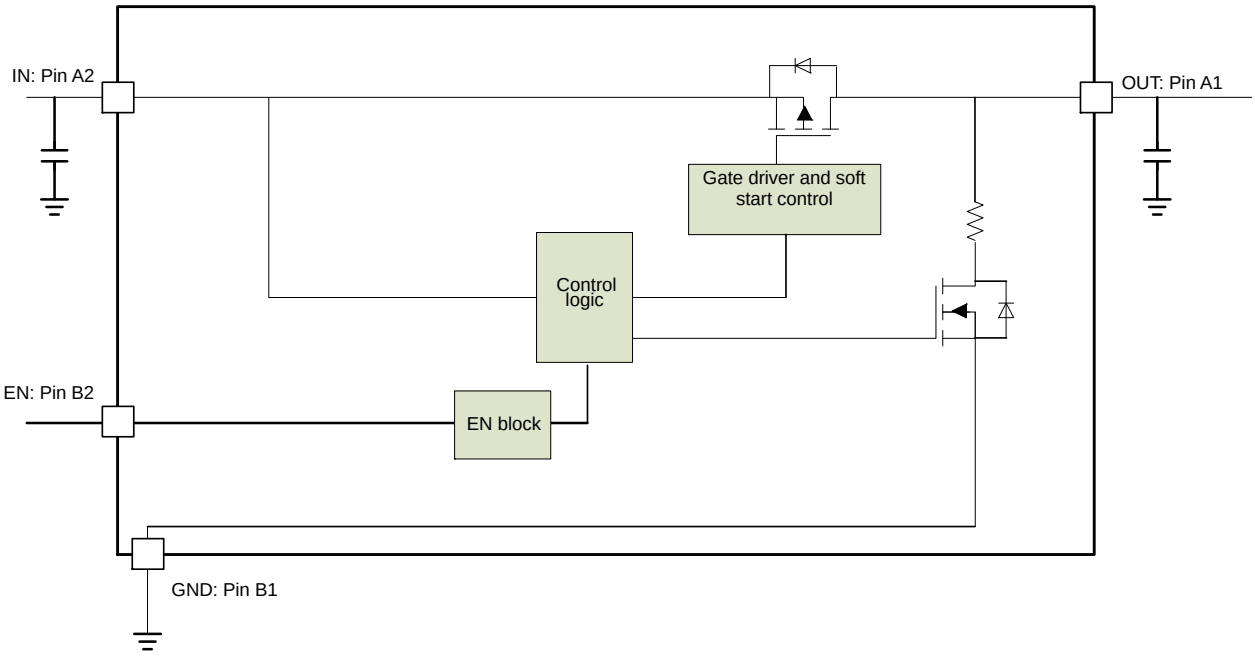


Figure 2. Block Diagram

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{EN}, V_{IN}, V_{OUT}	IN, OUT, EN, Pins	−0.3 to + 4.0	V
V_{IN}, V_{OUT}	From IN to OUT Pins: Input/Output	0 to + 4.0	V
ESD HBM	Human Body Model (HBM) ESD Rating are (Notes 1 and 2)	2500	V
ESD MM	Machine Model (MM) ESD Rating are (Notes 1 and 2)	250	V
ESD CDM	Charge Device Model (CDM) ESD Rating are (Notes 1 and 2)	2000	V
LU	Latch−up protection (Note 3) − Pins IN, OUT, EN	100	mA
T_J	Maximum Junction Temperature	−40 to + 125	°C
T_{STG}	Storage Temperature Range	−40 to + 150	°C
MSL	Moisture Sensitivity (Note 4)	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. According to JEDEC standard JESD22−A108.
2. This device series contains ESD protection and passes the following tests:
   Human Body Model (HBM) ±2.5 kV per JEDEC standard: JESD22−A114 for all pins.
   Machine Model (MM) ±250 V per JEDEC standard: JESD22−A115 for all pins.
   Charge Device Model (CDM) ±2.0 kV per JEDEC standard: JESD22−C101 for all pins.
3. Latch up Current Maximum Rating: ±100 mA per JEDEC standard: JESD78 class II.
4. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020.

OPERATING CONDITIONS

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IN}	Operational Power Supply			1.0		3.6	V
V_{EN}	Enable Voltage			0		3.6	
T_A	Ambient Temperature Range			−40	25	+ 85	°C
C_{IN}	Decoupling input capacitor			0.1			μF
C_{OUT}	Decoupling output capacitor			0.1			μF
$R_{\theta JA}$	Thermal Resistance Junction to Air	WLCSP package (Note 5)			100		°C/W
I_{OUT}	Maximum DC current					2	A
P_D	Power Dissipation Rating (Note 6)	$T_A \le 25°C$	WLCSP package		0.5		W
		$T_A = 85°C$	WLCSP package		0.2		

5. The $R_{\theta JA}$ is dependent of the PCB heat dissipation and thermal via.
6. The maximum power dissipation (P_D) is given by the following formula:

$$P_D = \frac{T_{JMAX} - T_A}{R_{\theta JA}}$$

ELECTRICAL CHARACTERISTICS Min and Max Limits apply for T_A between −40°C to +85°C for V_{IN} between 1.0 V to 3.6 V (Unless otherwise noted). Typical values are referenced to T_A = + 25 °C and V_{IN} = 3.3 V (Unless otherwise noted).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
POWER SWITCH							
$R_{DS(on)}$	Static drain−source on−state resistance	V_{IN} = 3.6 V	T_A = 25°C		27	34	mΩ
			T_J = 125°C			38	
		V_{IN} = 3.3 V	T_A = 25°C		28	35	
			T_J = 125°C			40	
		V_{IN} = 2.5 V	T_A = 25°C		31	39	
			T_J = 125°C			45	
		V_{IN} = 1.8 V	T_A = 25°C		37	45	
			T_J = 125°C			52	
		V_{IN} = 1.2 V	T_A = 25°C		54	70	
			T_J = 125°C			76	
		V_{IN} = 1.0 V	T_A = 25°C		73	95	
R_{DIS}	Output discharge path	EN = low	V_{IN} = 3.3 V	55	67	95	Ω
TIMINGS							
T_R	Output rise time	V_{IN} = 3.3 V	C_{LOAD} = 1 μF, R_{LOAD} = 25 Ω From 10% to 90% of V_{OUT}	40	75	160	μs
T_F	Output fall time		C_{LOAD} = 1 μF, R_{LOAD} = 25 Ω (Note 7)	10	50	80	μs
T_{dis}	Disable time		From EN vil to 90% V_{OUT}		8.7		μs
T_{on}	Gate turn on		Enable time + Output rise time	70	166	280	μs
T_{en}	Enable time		From EN low to high to V_{OUT} = 10% of fully on	30	66	120	μs
LOGIC PIN							
V_{IH}	High−level input voltage	V_{IN} = 3.3 V		0.90			V
V_{IL}	Low−level input voltage	V_{IN} = 3.3 V				0.5	V
QUIESCENT CURRENT							
I_Q	Current consumption	V_{IN} = 3.3 V, EN = low, No load			0.02	1	μA
		V_{IN} = 3.3 V, EN = high, No load			1.6	4	

7. Parameters are guaranteed for C_{LOAD} and R_{LOAD} connected to the OUT pin with respect to the ground
8. Guaranteed by design and characterization, not production tested.

TIMINGS

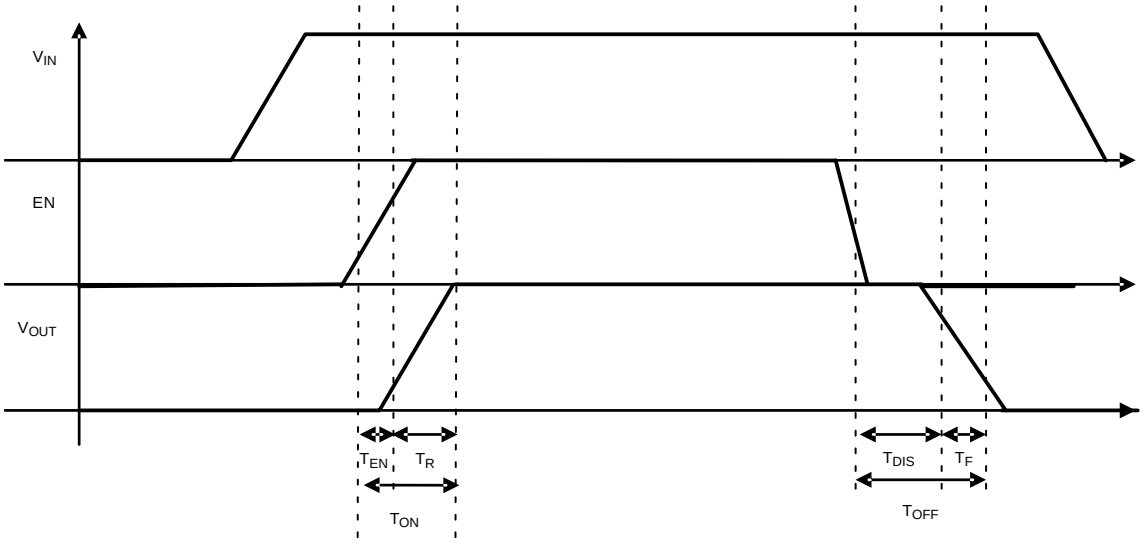


Figure 3. Enable, Rise and fall time

TYPICAL CHARACTERISTICS

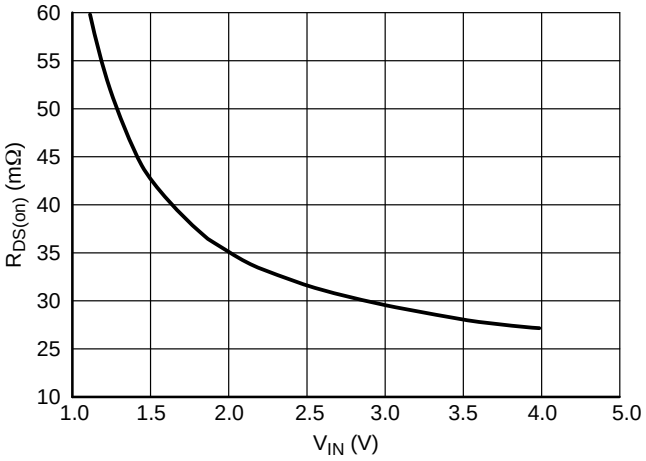


Figure 4. $R_{DS(on)}$ (mΩ) vs V_{IN} (V), No Load

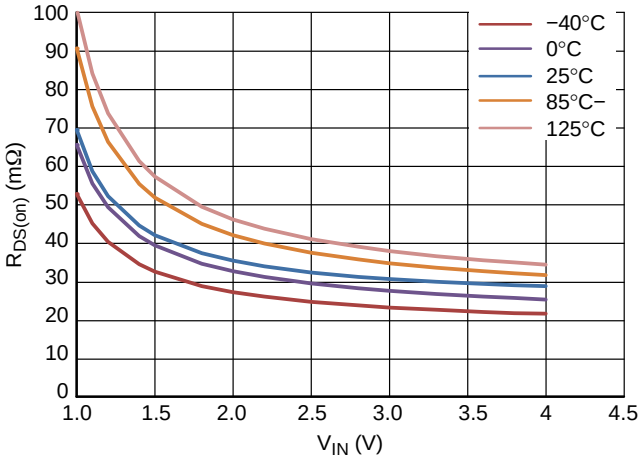


Figure 5. $R_{DS(on)}$ (mΩ) vs V_{IN} (V) In Temperature (°C), No Load

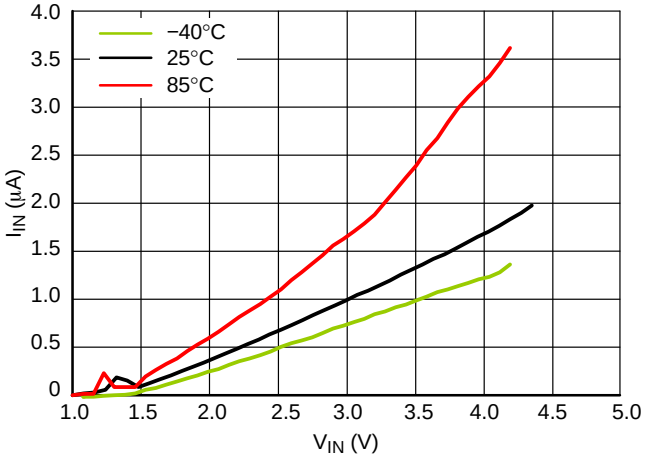


Figure 6. Quiescent Current (μA) vs V_{IN} (V), In Temperature

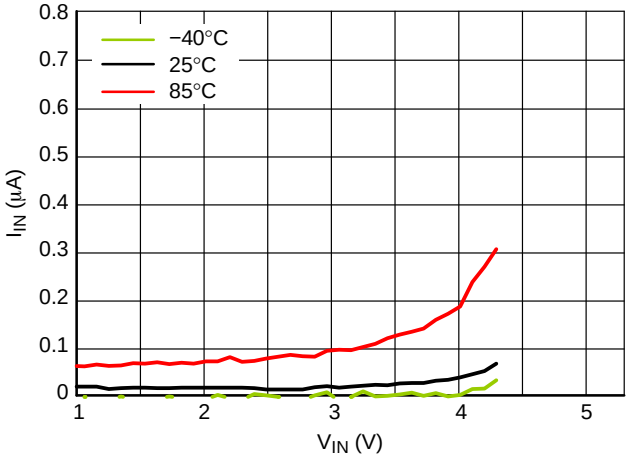


Figure 7. Standby Current (μA) vs V_{IN} (V), In Temperature

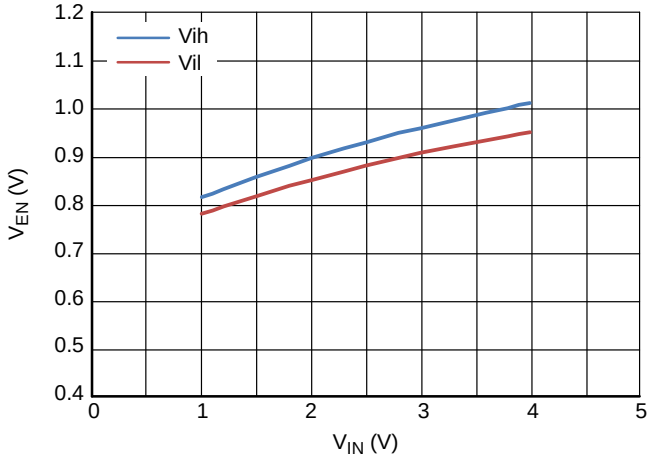


Figure 8. Enable Logic Threshold vs V_{IN}

FUNCTIONAL DESCRIPTION

Overview

The NCP439 is high side P channel MOSFET power distribution switch designed to isolate ICs connected on the battery in order to save energy. The part can be turned on, with a range of battery from 1.0 V to 3.6 V.

Enable input

Enable pin is an active high. The path is opened when EN pin is tied low (disable), forcing P MOS switch off.

The IN/OUT path is activated with a minimum of V_{IN} of 1.0 V and EN forced to high level.

Auto Discharge

N−MOSFET is placed between the output pin and GND, in order to discharge the application capacitor connected on OUT pin.

The auto−discharge is activated when EN pin is set to low level (disable state).

The discharge path (Pull down NMOS) stays activated as long as EN pin is set at low level and V_{IN} > 1.0 V.

In order to limit the current across the internal discharge N−MOSFET, the typical value is set at 65 Ω.

C_{IN} and C_{OUT} Capacitors

IN and OUT, 100 nF, at least, capacitors must be placed as close as possible the part for stability improvement.

APPLICATION INFORMATION

Power Dissipation

Main contributor in term of junction temperature is the power dissipation of the power MOSFET. Assuming this, the power dissipation and the junction temperature in normal mode can be calculated with the following equations:

$$P_D = R_{DS(on)} \times \left(I_{OUT}\right)^2$$

P_D = Power dissipation (W)
$R_{DS(on)}$ = Power MOSFET on resistance (Ω)
I_{OUT} = Output current (A)

$$T_J = P_D \times R_{\theta JA} + T_A$$

T_J = Junction temperature (°C)
$R_{\theta JA}$ = Package thermal resistance (°C/W)
T_A = Ambient temperature (°C)

PCB Recommendations

The NCP439 integrates an up to 2 A rated PMOS FET, and the PCB design rules must be respected to properly evacuate the heat out of the silicon. By increasing PCB area, especially around IN and OUT pins, the $R_{\theta JA}$ of the package can be decreased, allowing higher power dissipation.

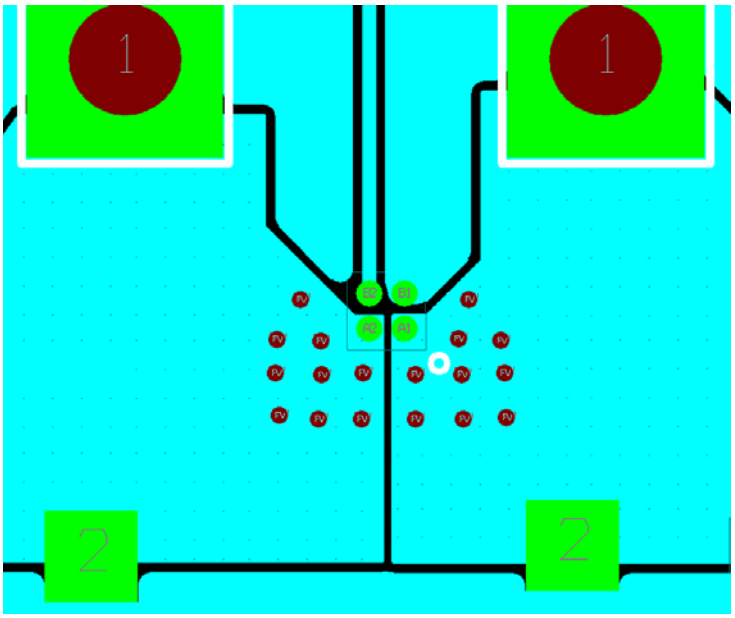


Figure 9. Routing Example 1 oz, 2 Layers, 100°C/W

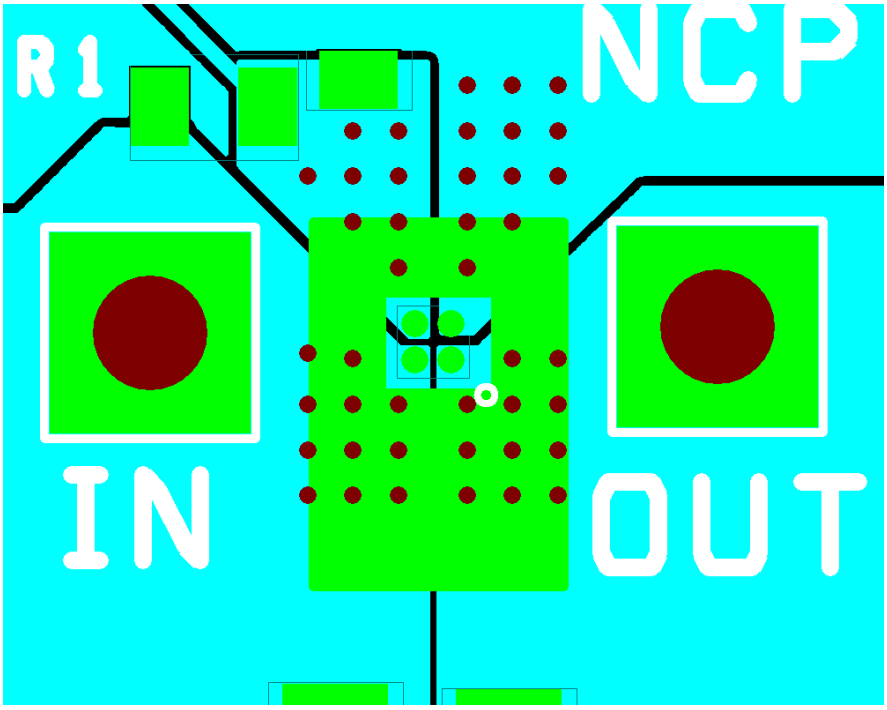


Figure 10. Routing Example 2 oz, 4 Layers, 60°C/W

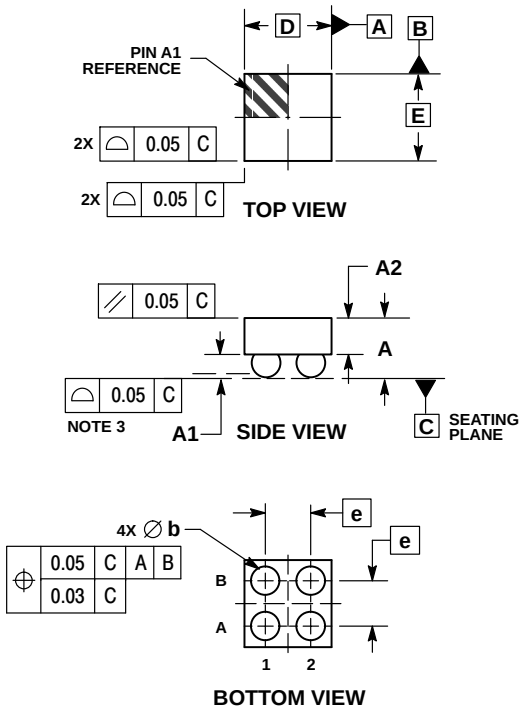
ORDERING INFORMATION

Device	Auto Discharge	Marking	Package	Shipping†
NCP439FCT2G	Yes	AY	WLCSP 0.96 x 0.96 mm (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

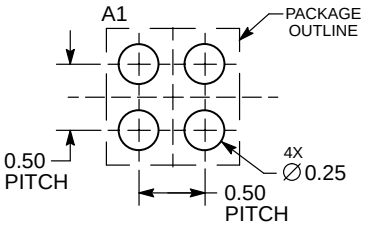
WLCSP4, 0.96x0.96
CASE 567FG
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.54	0.63
A1	0.22	0.28
A2	0.33 REF	
b	0.29	0.34
D	0.96 BSC	
E	0.96 BSC	
e	0.50 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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