Development Board EPC9003 Quick Start Guide

200 V Half-Bridge with Gate Drive, Using EPC2010

DESCRIPTION

The EPC9003 development board is a 200 V maximum device voltage, 5 A maximum output current, half bridge with onboard gate drives, featuring the EPC2010 enhancement mode (eGaN®) field effect transistor (FET). The purpose of this development board is to simplify the evaluation process of the EPC2010 eGaN FET by including all the critical components on a single board that can be easily connected into any existing converter.

The EPC9003 development board is 2″ x 1.5″ and contains not only two EPC2010 eGaN FET in a half bridge configuration with gate drivers, but also an on board gate drive supply and bypass capacitors. The board contains all critical components and layout for optimal switching performance. There are also various probe points to facilitate simple waveform measurement and efficiency calculation. A complete block diagram of the circuit is given in Figure 1.

For more information on the EPC2010s eGaN FET please refer to the datasheet available from EPC at www.epc-co.com. The datasheet should be read in conjunction with this quick start guide.

Table 1 **Performance Summary (T_A = 25°C)**

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{DD}	Gate Drive Input Supply Range		7	12	V
V_{IN}	Bus Input Voltage Range			150	V
V_{OUT}	Switch Node Output Voltage			200	V
I_{OUT}	Switch Node Output Current			5*	A
V_{PWM}	PWM Logic Input Voltage Threshold	Input 'High'	3.5	6	V
		Input 'Low'	0	1.5	V
	Minimum 'High' State Input Pulse Width	VPWM rise and fall time < 10ns	60		ns
	Minimum 'Low' State Input Pulse Width	VPWM rise and fall time < 10ns	500#		ns

*Assumes inductive load, maximum current depends on die temperature – actual maximum current with be subject to switching frequency, bus voltage and thermals.
Dependent on time needed to 'refresh' high side bootstrap supply voltage.

Quick Start Procedure

Development board EPC9003 is easy to set up to evaluate the performance of the EPC2010 eGaN FET. Refer to Figure 2 for proper connect and measurement setup and follow the procedure below:

1. With power off, connect the input power supply bus to +VIN (J5, J6) and ground / return to –VIN (J7, J8).
2. With power off, connect the switch node of the half bridge OUT (J3, J4) to your circuit as required.
3. With power off, connect the gate drive input to +VDD (J1, Pin-1) and ground return to –VDD (J1, Pin-2).
4. With power off, connect the input PWM control signal to PWM (J2, Pin-1) and ground return to any of the remaining J2 pins.
5. Turn on the gate drive supply – make sure the supply is between 7 V and 12 V range.
6. Turn on the bus voltage to the required value (do not exceed the absolute maximum voltage of 200 V on VOUT).
7. Turn on the controller / PWM input source and probe switching node to see switching operation.
8. Once operational, adjust the bus voltage and load PWM control within the operating range and observe the output switching behavior, efficiency and other parameters.
9. For shutdown, please follow steps in reverse.

NOTE. When measuring the high frequency content switch node (OUT), care must be taken to avoid long ground leads. Measure the switch node (OUT) by placing the oscilloscope probe tip through the large via on the switch node (designed for this purpose) and grounding the probe directly across the GND terminals provided. See Figure 3 for proper scope probe technique.

THERMAL CONSIDERATIONS

The EPC9003 development board showcases the EPC2010 eGaN FET. Although the electrical performance surpasses that for traditional Si devices, their relatively smaller size does magnify the thermal management requirements. The EPC9003 is intended for bench evaluation with low ambient temperature and convection cooling. The addition of heat-sinking and forced air cooling can significantly increase the current rating of these devices, but care must be taken to not exceed the absolute maximum die temperature of 125°C.

NOTE. The EPC9003 development board does not have any current or thermal protection on board.

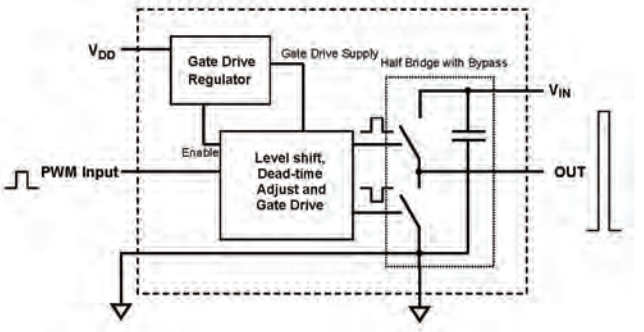


Figure 1: Block Diagram of EPC9003 Development Board

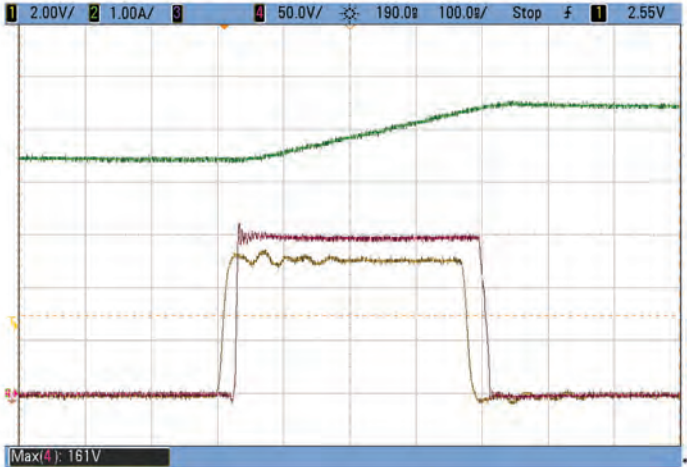


Figure 4: Waveforms for V_{IN} = 150 V to 5 V/5 A (100kHz) Buck converter
CH1: V_{PWM} Input voltage – CH2: (I_{OUT}) Switch node current – CH4: (V_{OUT}) Switch node voltage

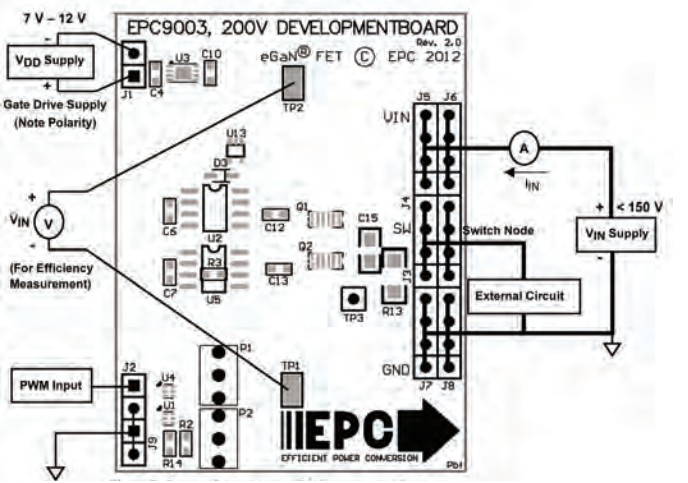


Figure 2: Proper Connection and Measurement Setup

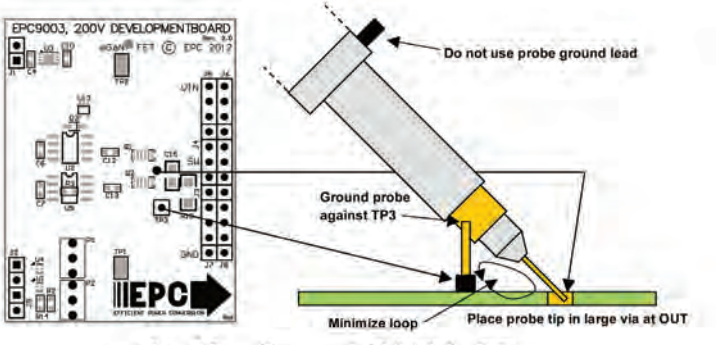
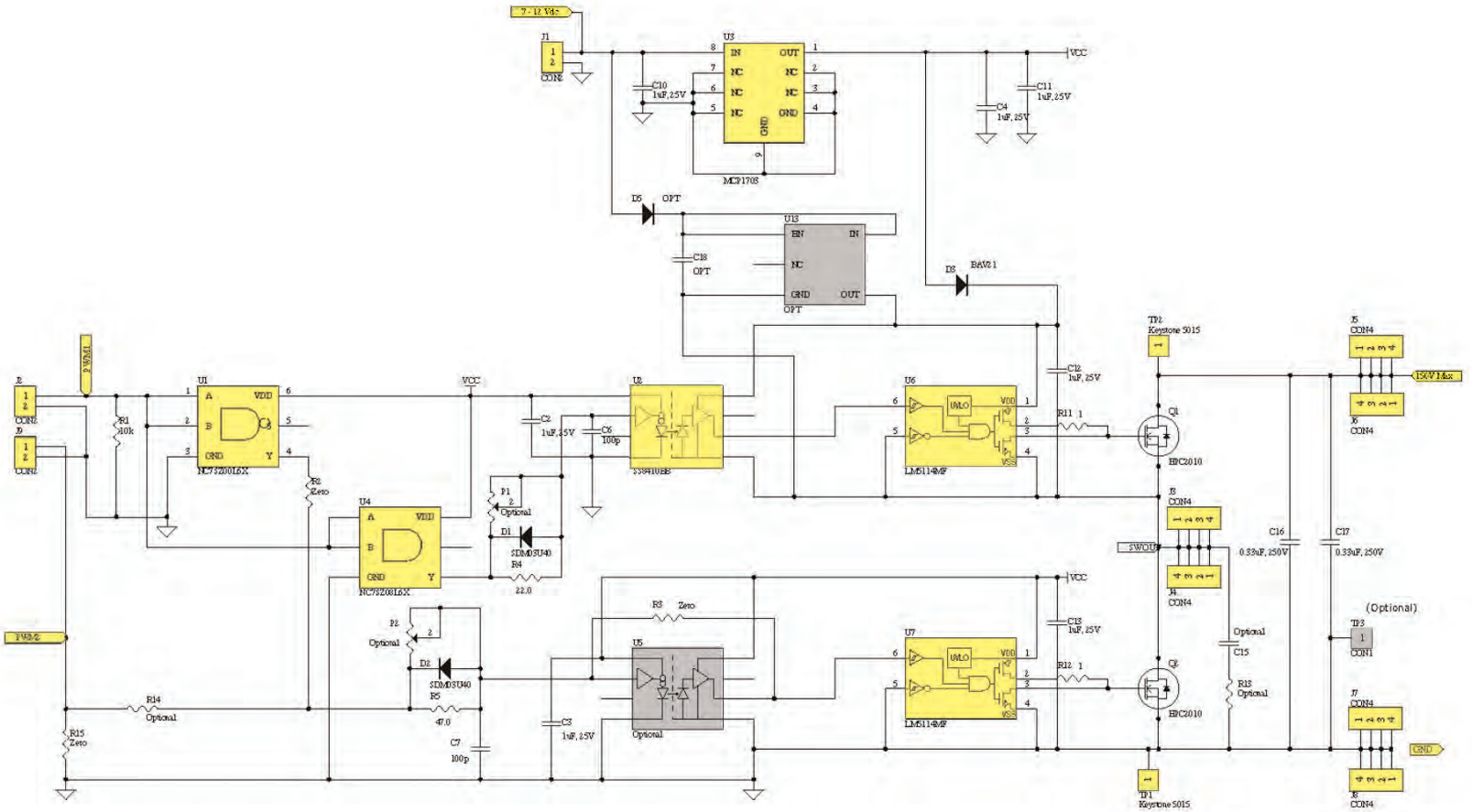


Figure 3: Proper Measurement of Switch Node – OUT

Table 2 : Bill of Material

Item	Qty	Reference	Part Description	Manufacturer / Part #
1	7	C2, C3, C4, C10, C11, C12, C13	Capacitor, 1uF, 10%, 25V, X5R	Murata, GRM188R61E105KA12D
2	2	C6, C7	Capacitor, 100pF, 5%, 50V, NP0	TDK, C1608C0G1H101J
3	2	C16, C17	Capacitor, .33UF, 20%, 250V, X7R	TDK, C4532X7R2E334M
4	2	D1, D2	Schottky Diode, 30V	Diodes Inc., SDM03U40-7
5	2	D3	Diode, 200V	Diodes Inc., BAV21WS-7-F
6	1	J1	Connector	2pins of Tyco, 4-103185-0
7	1	J2	Connector	4pins of Tyco, 4-103185-0
8	1	J3, J4, J5, J6, J7, J8	Connector	FCI, 68602-224HLF
9	2	Q1, Q2	eGaNFET	EPC, EPC2010
10	1	R1	*Resistor, 10.0K, 5%, 1/8W*	Stackpole, RMCF0603FT10K0
11	2	R11, R12	Resistor, 1 Ohm, 1%,1/8W	Stackpole, RMCF0603FT1R00
12	4	R2, R3, R4, R15	Resistor, 0 Ohm, 1/8W	Stackpole, RMCF0603FT00R0
13	1	R5	Resistor, TBD, 390 Ohm, 1%, 1/8W	Stackpole, RMCF0603FT390R
14	2	TP1, TP2	Test Point	Keystone Elect, 5015
15	1	TP3	Connector	1/40th of Tyco, 4-103185-0
16	1	U1	I.C., Logic	Fairchild, NC7SZ00L6X
17	1	U2	I.C., Opto-coupler	Silicon Labs, Si8410BB
18	1	U3	I.C., Regulator	Microchip, MCP1703T-5002E/MC
19	1	U4	I.C., Logic	Fairchild, NC7SZ08L6X
20	2	U6, U7	I.C., Gate driver	Texas Instruments, LM5114
21	0	C15, C18	Optional capacitor	
22	0	D5	Optional diode	
23	0	P1, P2	Optional Potentiometer	
24	0	R13, R14	Optional resistor	
25	0	U5, U13	Optional I.C.	



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Rev 2.0

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