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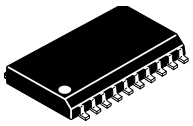
Switching Power Supply with Linear Regulators

33998

SWITCHING REGULATOR



DW SUFFIX
EG SUFFIX (PB-FREE)
98ASB42344B
24-PIN SOICW

The 33998 is a medium-power, multi-output power supply integrated circuit that is capable of operating over a wide input voltage range, from 6.0 V up to 26.5 V with 40 V transient capability. It incorporates a sensorless current mode control step-down switching controller regulating directly to 5.0 V. The 2.6 V linear regulator uses an external pass transistor to reduce the 33998 power dissipation. The 33998 also provides a 2.6 V linear standby regulator and two 5.0 V sensor supply outputs protected by internal low-resistance LDMOS transistors.

There are two separate enable pins for the main and sensor supply outputs and standard supervisory functions such as resets with power-up reset delay.

The 33998 provides proper power supply sequencing for advanced microprocessor architectures such as the MPC5xx and 683xx microprocessor families.

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MC33998DW/R2	-40°C to 125°C	24 SOICW
MCZ33998EG/R2		

Features

- Operating Voltage Range 6.0 V up to 26.5 V (40 V transient)
- Step-Down Switching Regulator Output V_{DDH} = 5.0 V @ 1400 mA (total)
- Linear Regulator with External Pass Transistor V_{DDL} = 2.6 V @ 400 mA
- Low-Power Standby Linear Regulator V_{KAM} = 2.6 V @ 10 mA
- Two 5.0 V @ 200 mA (typical) Sensor Supplies V_{REF} Protected Against Short-to-Battery and Short-to-Ground with Retry Capability
- Undervoltage Shutdown on the V_{DDL}, V_{DDH} Outputs with Retry Capability
- Reset Signals
- Power-Up Delay
- Enable Pins for Main Supplies (EN) and Sensor Supplies (SNSEN)
- Power Sequencing for Advanced Microprocessor Architectures
- Pb-Free Packaging Designated by Suffix Code EG

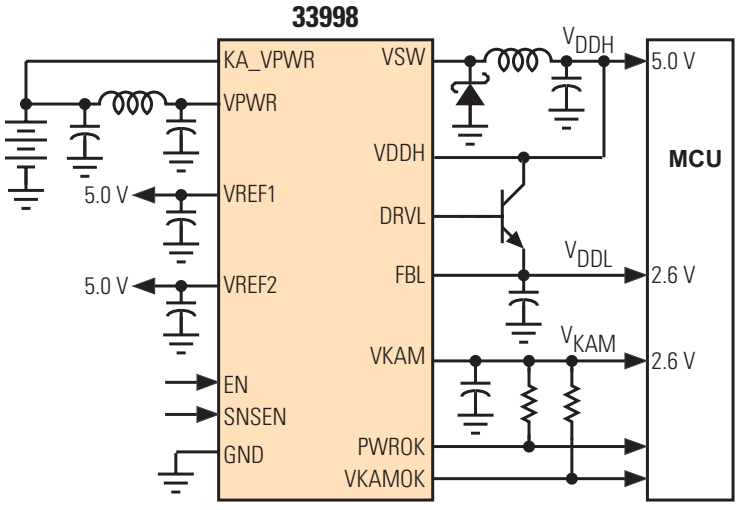


Figure 1. 33998 Simplified Application Diagram

INTERNAL BLOCK DIAGRAM

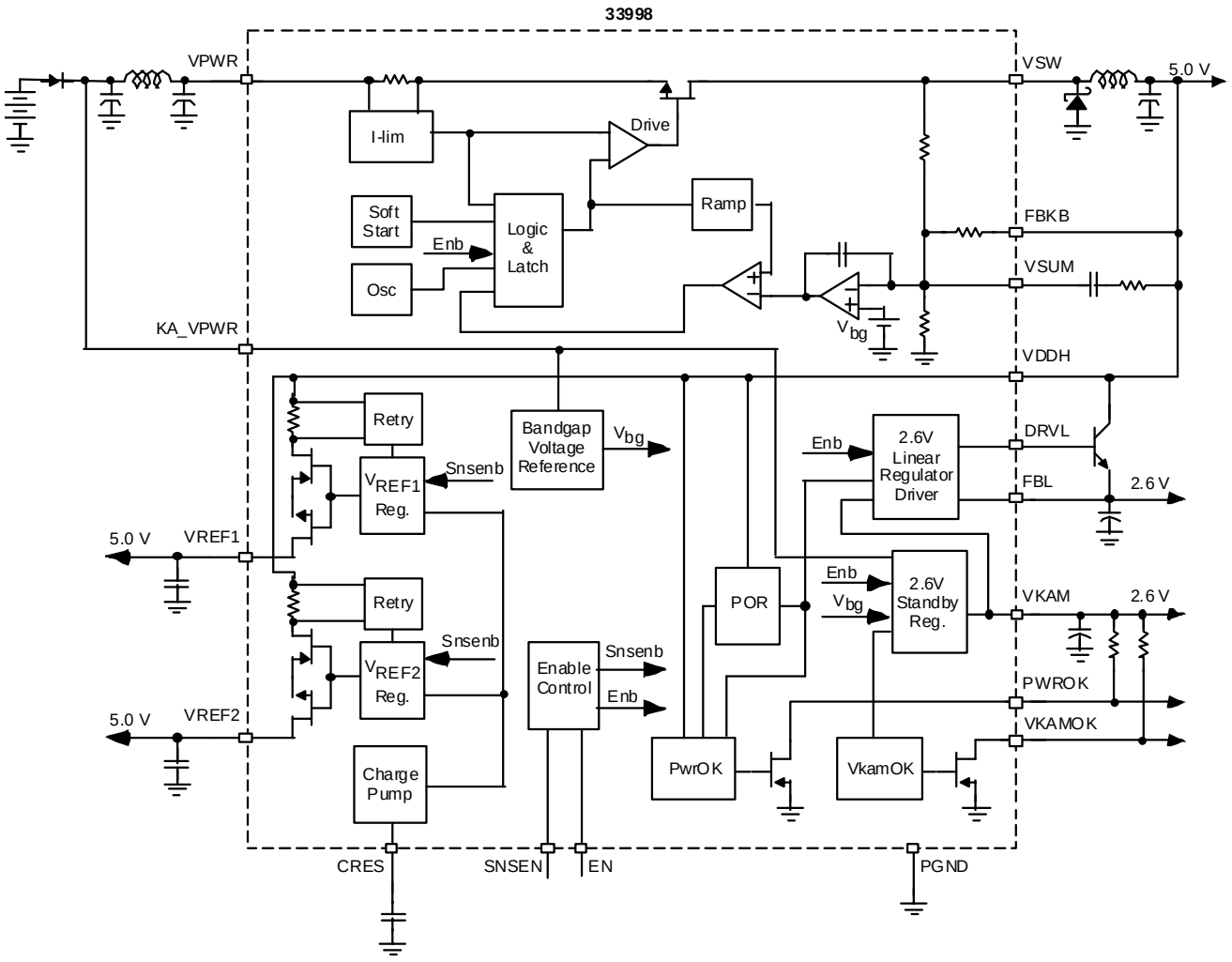


Figure 2. 33998 Simplified Internal Block Diagram

PIN CONNECTIONS

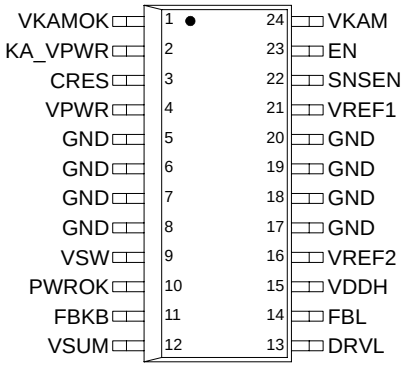


Figure 3. 33998 Pin Connections

Table 1. Pin Definitions

Pin Number	Pin Name	Definition
1	VKAMOK	Keep-Alive Output Monitoring. This pin is an "open-drain" output that will be used with a discrete pull-up resistor to VKAM. When the supply voltage to the 33998 is disconnected or lost, the VKAMOK signal goes low.
2	KA_VPWR	Keep Alive Power Supply Pin. This supply pin is used in modules that have both direct battery connections and ignition switch activated connections.
3	CRES	Reservoir Capacitor. This pin is tied to an external "reservoir capacitor" for the internal charge pump.
4	VPWR	Power Supply Pin. Main power input to the IC. This pin is directly connected to the switching regulator power MOSFET. In automotive applications this pin must be protected against reverse battery conditions by an external diode.
5–8	GND	Ground of the integrated circuit.
9	VSW	Internal P-Channel Power MOSFET Drain. VSW is the "switching node" of the voltage buck converter. This pin is connected to the VPWR pin by an integrated p-channel MOSFET.
10	PWROK	Power OK Reset Pin. This pin is an "open-drain" output that will be used with a discrete pull-up resistor to VKAM, VDDH, or VDDL. When either VDDH or VDDL output voltage goes out of the regulation limits this pin is pulled down.
11	FBKB	Step-Down Switching Regulator Feedback Pin. The FBKB pin is the VDDH feedback signal for the switching regulator.
12	VSUM	Error Amplifier "Summing Node". The VSUM pin is connected to the inverting input of the error amplifier. This node is also the "common" point of the integrated feedback resistor divider.
13	DRVL	Drive for VDDL (2.6 V) Regulator. The DRVL pin drives the base of an external NPN pass transistor for the VDDL linear post regulator. The collector of the VDDL pass transistor is connected to VDDH. An example of a suitable pass transistor is BCP68.
14	FBL	Feedback for VDDL (2.6 V) Regulator. The FBL pin is the voltage feedback sense signal from the VDDL (2.6 V) linear post regulator.
15	VDDH	VDDH is an input supply pin providing power for the buffered sensor supplies and the drive circuitry for the 2.6 V linear power regulator. The VDDH pin is supplied from the switching regulator output, capable of providing 5.0 V @ 1400 mA total output current.
16	VREF2	Sensor Supply #2 Output. The VREF2 pin is sensor supply output #2.
17–20	GND	Ground of the integrated circuit.
21	VREF1	Sensor Supply #1 Output. The VREF1 pin is sensor supply output #1.

Table 1. Pin Definitions (continued)

Pin Number	Pin Name	Definition
22	SNSEN	Sensor Supply Enable Input. The SNSEN pin is an input, which enables the VREF1 and VREF2 supplies. It allows the control module hardware/software to shut down the sensor supplies.
23	EN	Enable Input. The EN pin is an input, which enables the main switching regulator and all other functions. When this pin is low, the power supply is in a low quiescent state.
24	VKAM	Keep-Alive (standby) 2.6 V Regulator Output. This is a 2.6 V low quiescent, low dropout regulator for Keep Alive memory.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
Main Supply Voltage	V_{PWR}	-0.3 to 45	V
Keep-Alive Supply Voltage	KA_V_{PWR}	-0.3 to 45	V
Switching Node	V_{SW}	-0.5 to 45	V
5.0 V Input Power	V_{DDH}	-0.3 to 6.0	V
Sensor Supply	V_{REF1} V_{REF2}	-0.3 to 18 -0.3 to 18	V
Keep-Alive Supply Voltage	V_{KAM}	-0.3 to 6.0	V
Maximum Voltage at Logic I/O Pins	EN SNSEN PWROK VKAMOK	-0.3 to 6.0 -0.3 to 6.0 -0.3 to 6.0 -0.3 to 6.0	V
Charge Pump Reservoir Capacitor Voltage	C_{RES}	-0.3 to 18	V
Error Amplifier Summing Node	V_{SUM}	-0.3 to 6.0	V
Switching Regulator Output Feedback	FBKB	-0.3 to 6.0	V
VDDL Base Drive	DRVL	-0.3 to 6.0	V
VDDL Feedback	FBL	-0.3 to 6.0	V
ESD Voltage Human Body Model (all pins) (1) Machine Model (all pins) (1)	 V_{ESD1} V_{ESD2}	 ±500 ±100	V
Power Dissipation (T_A = 25°C) (2)	P_D	800	mW
Thermal Resistance, Junction to Ambient (3), (4)	$R_{\theta JA}$	60	°C/W
Thermal Resistance, Junction to Board (5)	$R_{\theta JB}$	20	°C/W
Operational Package Temperature [Ambient Temperature] (6)	T_A	-40 to 125	°C

Notes

1. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP}=100 pF, R_{ZAP}=1500 Ω). ESD2 testing is performed in accordance with the Machine Model (C_{ZAP}=200 pF, R_{ZAP}=0 Ω)
2. Maximum power dissipation at indicated junction temperature.
3. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
4. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
5. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
6. The limiting factor is junction temperature, taking into account the power dissipation, thermal resistance, and heat sinking.

Table 2. Maximum Ratings (continued)

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
Operational Junction Temperature	T_J	-40 to 150	°C
Storage Temperature	T_{STG}	-55 to 150	°C
Peak Package Reflow Temperature During Reflow (7), (8)	T_{PPRT}	Note 8	°C

7. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
8. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL),
Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 9.0 V ≤ V_{PWR} ≤ 16 V, -40°C ≤ T_J = T_A ≤ 125°C, using the typical application circuit (see Figure 8) unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
GENERAL					
Supply Voltage Range					V
Normal Operating Voltage Range (9)	$V_{PWR(N)}$	6.0	–	18	
Extended Operating Voltage Range (9)	$V_{PWR(E)}$	18	–	26.5	
Maximum Transient Voltage - Load Dump (10)	$V_{PWR(LD)}$	–	–	40	V
VPWR Supply Current EN = 5.0 V, V_{PWR} = 14 V, No Loads	I_{VPWR}	25	–	150	mA
VPWR Quiescent Supply Current EN = 0 V, V_{PWR} = 12 V	I_{QVPWR}	5.0	–	15	μA
KA_VPWR Supply Current, EN = 5.0 V, KA_V_{PWR} = 14 V, No Load on V_{KAM}	I_{KAVPWR}	0.5	–	3.0	mA
KA_VPWR Quiescent Supply Current EN = 0 V, KA_V_{PWR} = 12 V	$I_{QKAVPWR}$	50	–	350	μA
BUCK REGULATOR (VDDH)					
Buck Converter Output Voltage I_{VDDH} = 200 mA to 1.4 A, V_{PWR} = KA_V_{PWR} = 14 V	V_{DDH}	4.9	–	5.1	V
Buck Converter Output Voltage I_{VDDH} = 1.4 A, V_{PWR} = KA_V_{PWR} = 6.0 V	V_{DDH}	4.9	–	5.1	V
VDDH Line Regulation V_{PWR} = KA_V_{PWR} = 10 V to 14 V, I_{VDDH} = 200 mA	$REGLN_{VDDH}$	-20	–	30	mV
VDDH Load Regulation					mV
V_{PWR} = KA_V_{PWR} = 14 V, I_{VDDH} = 200 mA to 1.4 A	$REGLD_{VDDH}$	-20	–	20	
V_{PWR} = KA_V_{PWR} = 6.0 V, I_{VDDH} = 200 mA to 1.4 A		-20	–	20	
VDDH Active Discharge Resistance V_{PWR} = KA_V_{PWR} = 14 V, EN = 0 V, I_{VDDH} = 10 mA	R_{HDISCH}	1.0	–	15	Ω
P-CHANNEL MOSFET					
Drain-Source Breakdown Voltage—Not Tested (11)	BV_{DSS}	45	–	–	V
Drain-Source Current Limit—Not Tested (11)	ISC_{SW1}	–	-7.0	–	A

Notes

9. VDDH is fully functional when the 33998 is operating at higher battery voltages, but these parameters are not tested. The test condition as are:
   a) V_{DDH} must be between 4.9 V and 5.1 V (200 mA to 1.4 A) for V_{PWR} = 14 V to 18 V.
   b) V_{DDH} must be between 4.8 V and 5.5 V (200 mA to 1.4 A) for V_{PWR} = 18 V to 26.5 V.
10. Part can survive, but no parameters are guaranteed.
11. Guaranteed by design but not production tested.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 9.0 V ≤ V_{PWR} ≤ 16 V, -40°C ≤ T_J = T_A ≤ 125°C, using the typical application circuit (see Figure 8) unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LINEAR REGULATOR (VDDL)					
VDDL Output Voltage V_{PWR} = KA_V_{PWR} = 14 V, I_{VDDL} = 200 mA	V_{DDL}	2.5	2.6	2.7	V
VDDL Line Regulation V_{DDH} = 4.8 V to 5.2 V, I_{VDDL} = 400 mA	$REGLN_{VDDL}$	-30	–	30	mV
VDDL Load Regulation V_{PWR} = KA_V_{PWR} = 14 V, I_{VDDL} = 10 mA to 400 mA	$REGLD_{VDDL}$	-70	–	70	mV
DRVL Output Current V_{PWR} = KA_V_{PWR} = 14 V, VDRVL = 1.0 V	I_{DRVL}	5.0	11	25	mA
VDDL Active Discharge Resistance V_{PWR} = KA_V_{PWR} = 14 V, EN = 0 V, I_{FBL} = 10 mA	R_{LDISCH}	1.0	–	10	Ω
VDDH to VDDL Active Clamp Resistance V_{PWR} = KA_V_{PWR} = 14 V, EN = 0 V, I_{VDDH} = 50 mA, V_{FBKB} = 0 V	R_{CLAMP}	0.6	–	10	Ω
VDDL Output Capacitor Capacitance (12)	C_{VDDL}	–	68	–	µF
VDDL Output Capacitor ESR (12)	ESR_{VDDL}	–	0.125	–	Ω
KEEP-ALIVE (STANDBY) REGULATOR (VKAM)					
VKAM Output Voltage I_{VKAM} = 5.0 mA, VPWR = KA_V_{PWR} = 18 V, EN = 5.0 V	V_{KAM}	2.5	–	2.7	V
VKAM Output Voltage, EN = 0 V (Standby Mode) V_{PWR} = KA_V_{PWR} = 26 V, I_{VKAM} = 0.5 mA V_{PWR} = KA_V_{PWR} = 18 V, I_{VKAM} = 5.0 mA V_{PWR} = KA_V_{PWR} = 5.0 V, I_{VKAM} = 10.0 mA V_{PWR} = 0 V, KA_V_{PWR} = 3.5 V, I_{VKAM} = 5.0 mA	V_{KAM}	2.5 2.5 2.5 2.0	– – – –	2.7 2.7 2.7 2.7	V
VKAM Line Regulation, EN = 0 V (Standby Mode) V_{PWR} = KA_V_{PWR} = 5.0 V to 18 V, I_{VKAM} = 2.0 mA	$REGLN_{VKAM}$	-20	–	20	mV
VKAM Load Regulation, EN = 0 V (Standby Mode) V_{PWR} = KA_V_{PWR} = 14 V, I_{VKAM} = 1.0 mA to 10 mA	$REGLDD_{VKAM}$	0	–	100	mV
Differential Voltage V_{KAM} - V_{DDL} EN = 5.0 V, I_{VKAM} = 5.0 mA, V_{PWR} = KA_V_{PWR} = 14 V, I_{VDDL} = 200 mA	REG_{VKAM}	-20	–	60	mV
VKAM Output Capacitor Capacitance (12)	C_{VKAM}	–	4.7	–	µF
VKAM Output Capacitor ESR (12)	ESR_{VKAM}	–	1.4	–	Ω

Notes
12. Recommended value.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 9.0 V ≤ V_{PWR} ≤ 16 V, -40°C ≤ T_J = T_A ≤ 125°C, using the typical application circuit (see Figure 8) unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SENSOR SUPPLIES (VREF1, VREF2)					
VREF On-Resistance, T_A = -40°C I_{VREF} = 200 mA, I_{VDDH} = 200 mA, V_{PWR} = KA_V_{PWR} = 14 V, EN = 5.0 V	$R_{DS(ON)}$	–	–	280	mΩ
VREF On-Resistance, T_A = +25°C I_{VREF} = 200 mA, I_{VDDH} = 200 mA, V_{PWR} = KA_V_{PWR} = 14 V, EN = 5.0 V	$R_{DS(ON)}$	–	–	350	mΩ
VREF On-Resistance, T_A = +125°C I_{VREF} = 200 mA, I_{VDDH} = 200 mA, V_{PWR} = KA_V_{PWR} = 14 V, EN = 5.0 V	$R_{DS(ON)}$	–	–	455	mΩ
VREF Short-to-Battery Detect Current V_{PWR} = KA_V_{PWR} = 14 V, EN = 5.0 V, SNSEN = 5.0 V	I_{SC_BAT}	500	–	900	mA
VREF Short-to-Ground Detect Current V_{PWR} = KA_V_{PWR} = 14 V, EN = 5.0 V, SNSEN = 5.0 V	I_{SC_GND}	500	–	900	mA
Maximum Output Capacitance (Total) (13)	C_{VREF}	33	–	39	nF
SUPERVISORY CIRCUITS (VPWR)					
PWROK Undervoltage Threshold on V_{DDL}, FBL Ramps Down V_{PWR} = KA_V_{PWR} = 14 V, I_{VDDH} = 200 mA	$V_{FBL(THL)}$	2.1	2.4	2.5	V
PWROK Undervoltage Threshold on V_{DDH} V_{PWR} = KA_V_{PWR} = 14 V, I_{VDDH} = 200 mA	$V_{DDH(THL)}$	4.5	–	4.8	V
VDDH Overvoltage Threshold V_{PWR} = KA_V_{PWR} = 10 V, I_{VDDH} = 200 mA	$V_{DDH(THH)}$	5.12	–	5.7	V
PWROK Open Drain On-Resistance V_{PWR} = KA_V_{PWR} = 14 V, EN = 5 V, I_{PwrOK} = 5.0 mA	$R_{DS(ON)}$	–	–	200	Ω
VKAMOK Threshold, V_{PWR} = KA_V_{PWR} = 14 V, I_{VDDH} = 200 mA	$V_{KAM(THL)}$	2.1	2.4	2.5	V
VKAMOK Threshold on V_{PWR}, V_{PWR} Ramps Up KA_V_{PWR} = 14 V, I_{VDDH} = 200 mA	$V_{PWROK(TH)}$	4.0	–	5.0	V
VKAMOK Open Drain On-Resistance V_{PWR} = KA_V_{PWR} = 14 V, EN = 0 V, I_{VKAMOK} = 10 mA	$R_{DS(ON)}$	50	–	200	Ω
Enable Input Voltage Threshold (Pin EN)	V_{IH}	1.0	–	2.0	V
Enable Pull-Down Current (Pin EN), EN = 1.0 V V_{DDH} to $V_{IL(MIN)}$	I_{PD}	500	–	1200	nA
Sensor Enable Input Voltage Threshold (Pin SNSEN)	V_{IH}	1.0	–	2.0	V
Sensor Enable Pull-Down Current (Pin SNSEN) SNSEN = 1.0 V V_{DDH} to $V_{IL(MIN)}$	I_{PD}	500	–	1200	nA

Notes

13. Recommended value.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 9.0 V ≤ V_{PWR} ≤ 16 V, -40°C ≤ T_J = T_A ≤ 125°C, using the typical application circuit (see Figure 8) unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CHARGE PUMP (CRES)					
Charge Pump Voltage	V_{CRES}				V
V_{PWR} = KA_V_{PWR} = 14 V, I_{VDDH} = 200 mA, I_{CP} = 0 μA		12	–	15	
V_{PWR} = KA_V_{PWR} = 14 V, I_{VDDH} = 200 mA, I_{CP} = 10 μA		12	–	15	

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions 9.0 V ≤ V_{PWR} ≤ 16 V, -40°C ≤ T_J = T_A ≤ 125°C using the typical application circuit (see Figure 8) unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
BUCK REGULATOR (VDDH)					
Switching Frequency (14)	f_{SW}	–	750	–	kHz
Soft Start Duration (see Figure 2) V_{PWR} = KA_V_{PWR} = 6.0 V	t_{SS}	5.0	–	15	ms
CHARGE PUMP (CRES)					
Charge Pump Current Ramp-Up Time V_{PWR} = KA_V_{PWR} = 14 V, C_{RES} = 22 nF, V_{CP} = 1.0 V to 11 V	t_{CRES}	1.0	–	20	ms
Charge Pump Ramp-Up Time V_{PWR} = KA_V_{PWR} = 7.0 V, C_{RES} = 22 nF, V_{CP} = 7.0 V to 10 V	t_{CRES}	1.0	–	10	ms
SENSOR SUPPLIES (VREF1, VREF2)					
VREF Overcurrent Detection Time (see Figure 3) V_{REF} Load R_L = 5.0 Ω to GND, V_{DDH} = 5.1 V, V_{PWR} = KA_V_{PWR} = 10 V, EN = 5.0 V, SNSEN = 5.0 V	t_{DET}	0.5	–	2.0	µs
VREF Retry Timer Delay (see Figure 3) V_{REF} Load R_L = 5.0 Ω to GND, V_{DDH} = 5.1 V, V_{PWR} = KA_V_{PWR} = 10 V, EN = 5.0 V, SNSEN = 5.0 V	t_{RET}	5.0	–	20	ms
SUPERVISORY CIRCUITS (VPWR)					
PWROK Delay Time (Power-On Reset) (see Figure 4)	$t_{D(PWROK)}$	5.0	–	15	ms
VKAMOK Delay Time (see Figure 5)	$t_{D(VKAMOK)}$	10	–	30	ms
VDDH Power-Up Delay Time (see Figure 6)	$t_{D(VPWR)}$	1.0	–	10	ms
Fault-Off Timer Delay Time (see Figure 7)	t_{FAULT}	1.0	–	10	ms

Notes

14. Guaranteed by design but not production tested.

TIMING DIAGRAMS

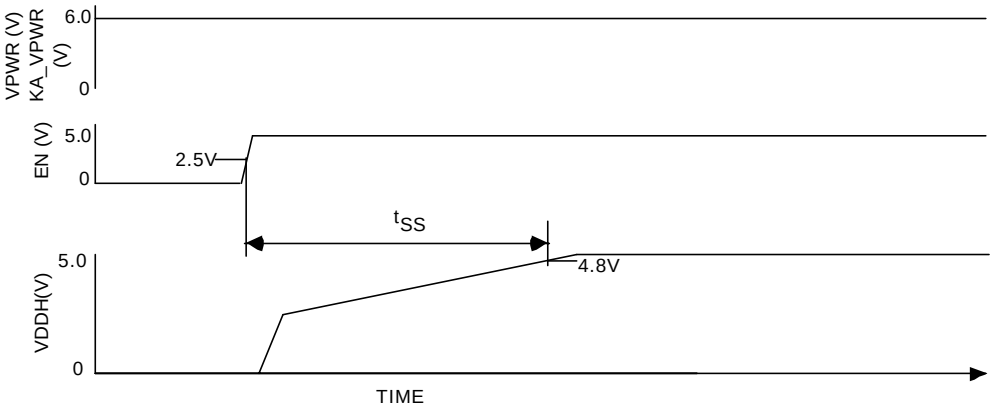


Figure 4. Soft-Start Time

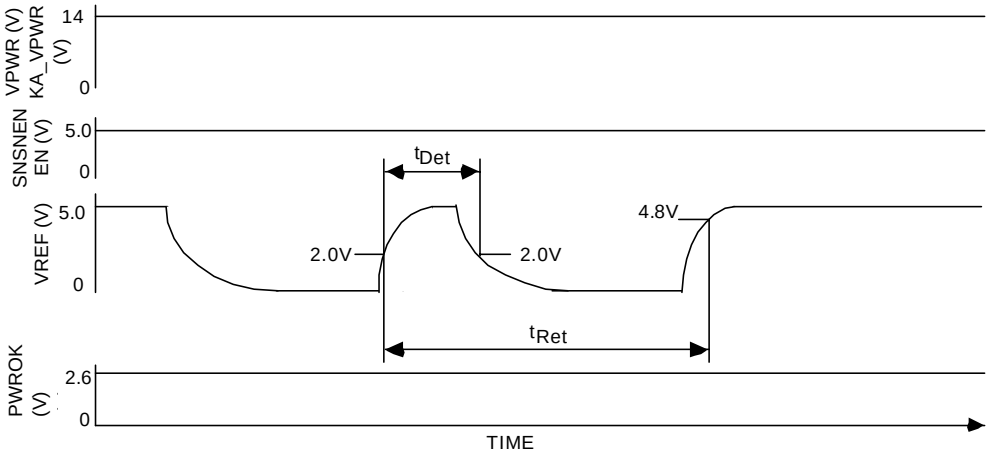


Figure 5. VREF Retry Timer

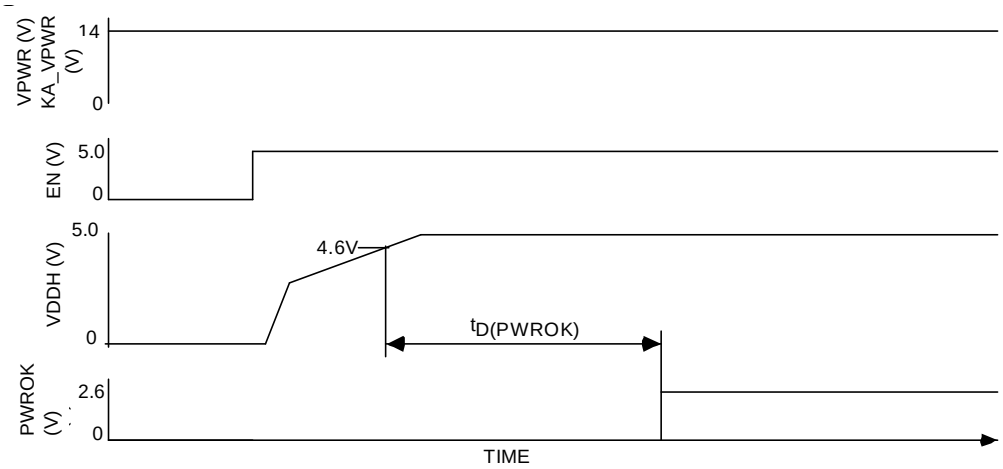


Figure 6. PWROK Delay Timer (Power-On Reset)

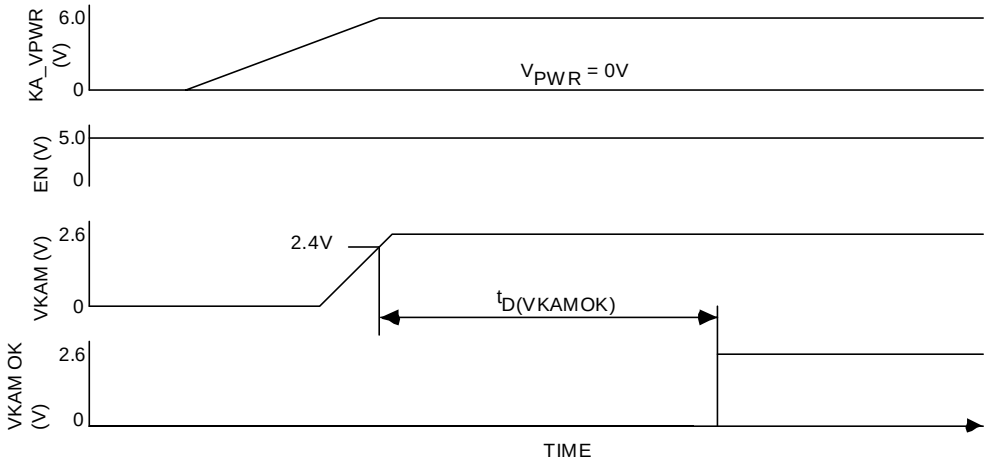


Figure 7. VKAMOK Delay Time

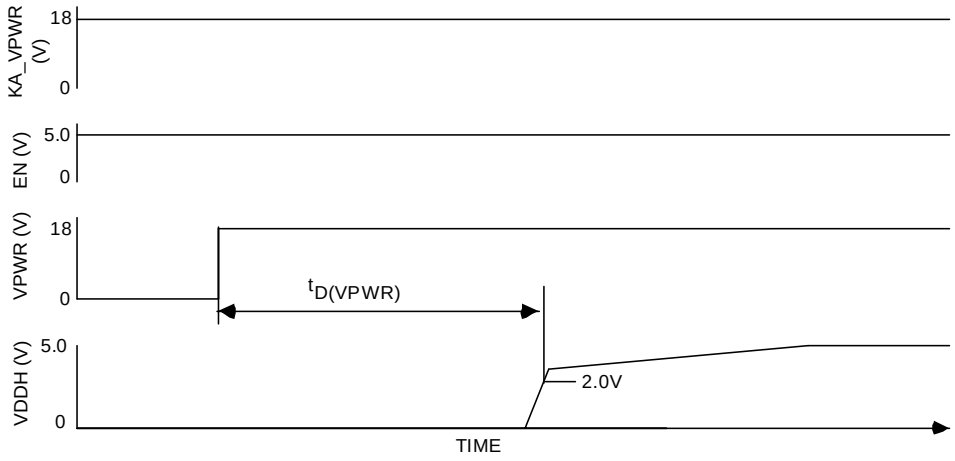


Figure 8. VDDH Power-Up Delay Time

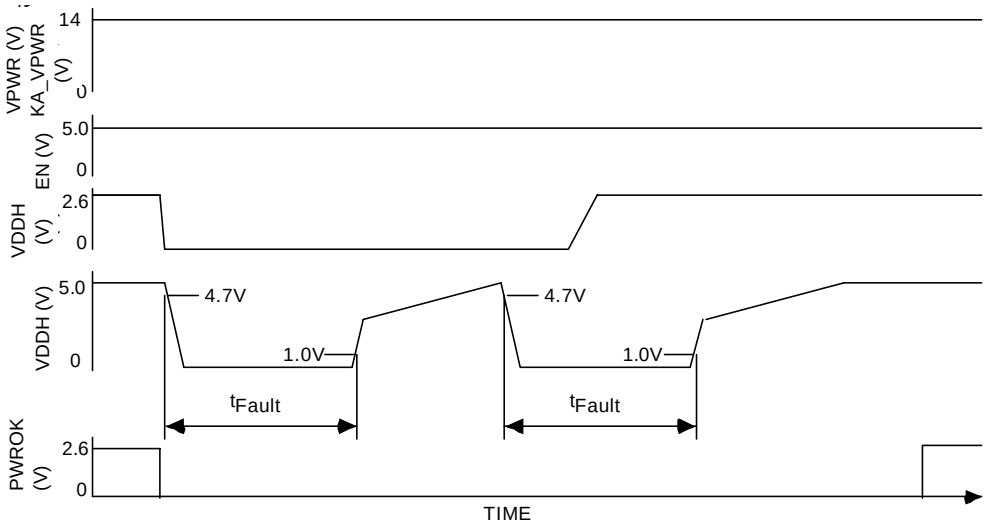


Figure 9. Fault-Off Timer Delay Time

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33998 multi-output power supply integrated circuit is capable of operating from 6.0 V up to 26.5 V with 40 V transient capability. It incorporates a step-down switching controller regulating directly to 5.0 V. The 2.6 V linear regulator uses an external pass transistor, thus reducing the power dissipation of the integrated circuit. The 33998 also provides a 2.6 V linear standby regulator and two 5.0 V sensor supply outputs protected by internal low-resistance LDMOS transistors against short-to-battery and short-to-ground.

FUNCTIONAL PIN DESCRIPTION

SWITCHING REGULATOR (VDDH)

The switching regulator is a high-frequency (750 kHz), conventional buck converter with integrated high-side p-channel power MOSFET. Its output voltage is regulated to provide 5.0 V with ±2% accuracy and it is intended to directly power the digital and analog circuits of the Electronic Control Module (ECM). The switching regulator output is rated for 1400 mA total output current. This current can be used by the linear regulator VDDL and sensor supplies VREF1 and VREF2. The 33998 switching controller utilizes "Sensorless Current Mode Control" to achieve good line rejection and stabilize the feedback loop. A soft-start feature is incorporated into the 33998. When the device is enabled, the switching regulator output voltage VDDH ramps up to about half of full scale and then takes 16 steps up to the nominal regulation voltage level (5.0 V nominal).

2.6 V LINEAR REGULATOR (VDDL)

The 2.6 V linear post-regulator is powered from the 5.0 V switching regulator output (VDDH). A discrete pass transistor is used to the power path for the VDDL regulator. This arrangement minimizes the power dissipation off the controller IC. The FBL pin is the feedback input of the regulator control loop and the DRVL pin the external NPN pass transistor base drive. Power up, power down, and fault management are coordinated with the 5.0 V switching regulator.

SENSOR SUPPLIES (VREF1) AND (VREF2)

The sensor supplies are implemented using a protected switch to the main 5.0 V (switching regulator) output. The 33998 integrated circuit provides two low-resistance LDMOS power MOSFETs connected to the switching regulator output (VDDH). These switches have short-to-battery and short-to-ground protection integrated into the IC. When a severe fault conditions is detected, the affected sensor output is turned off and the sensor Retry Timer starts to time out. After the Retry Timer expires, the sensor supply tries to power up again. Sensor supplies VREF can be disabled by pulling the Sensor Enable SNSEN pin low (see Figure 7 for the VREF Retry Timer operation).

Notes: Severe fault conditions on the VREF1 and VREF2 outputs, like hard shorts to either ground or battery, may disrupt the operation of the main regulator VDDH. Shorts to battery above 17 V are considered “double faults” and neither one of the VREF outputs is protected against such conditions.

Depending on the VDDH capacitor value and its ESR value, the severity of the short may disrupt the VDDH operation.

KEEP-ALIVE REGULATOR, *STANDBY (*VKAM)

The Keep-Alive Regulator VKAM (keep-alive memory) is intended to provide power for “key off” functions such as nonvolatile SRAM, “KeyOff" timers and controls, KeySwitch monitor circuits, and perhaps a CAN/SCP monitor and wake-up function. It may also power other low-current circuits required during a “KeyOff” condition. The regulated voltage is nominally 2.6 V. A severe fault condition on the VKAM output is signaled by pulling the VKAMOK signal low.

KEEP-ALIVE OPERATION, *STANDBY, POWER-DOWN MODE* (VKAM)

When the EN pin is pulled low, the power supply is forced into a low-current standby mode. In order to reduce current drawn by the VPWR and KA_VPWR pins, all power supply functions are disabled except for the VKAM and Enable (EN) pins. The latter pin is monitored for the "wake-up" signal. The switching transistor gate is actively disabled and the VDDL and VDDH pins are actively pulled low.

POWER-UP DELAY TIMERS

Two Power-Up Delay timers are integrated into the control section of the integrated circuit. One timer monitors the input voltage at the VPWR input pin (see Figure 3), and the other monitors the input voltage at the KA_VPWR input pin. In both cases, sufficient supply voltage must be present long enough for the timers to “time out” before the switching regulator can be enabled.

FAULT-OFF TIMER

If the VDDL output voltage does not reach its valid range at the end of soft-start period, or if the VDDH or VDDL output voltage gets below its PWROK threshold level, the Fault-Off Timer shuts the switching regulator off until the timer “times out” and the switching regulator retries to power up again (see Figure 7 for Fault-Off Timer operation details).

POWER-ON RESET TIMER

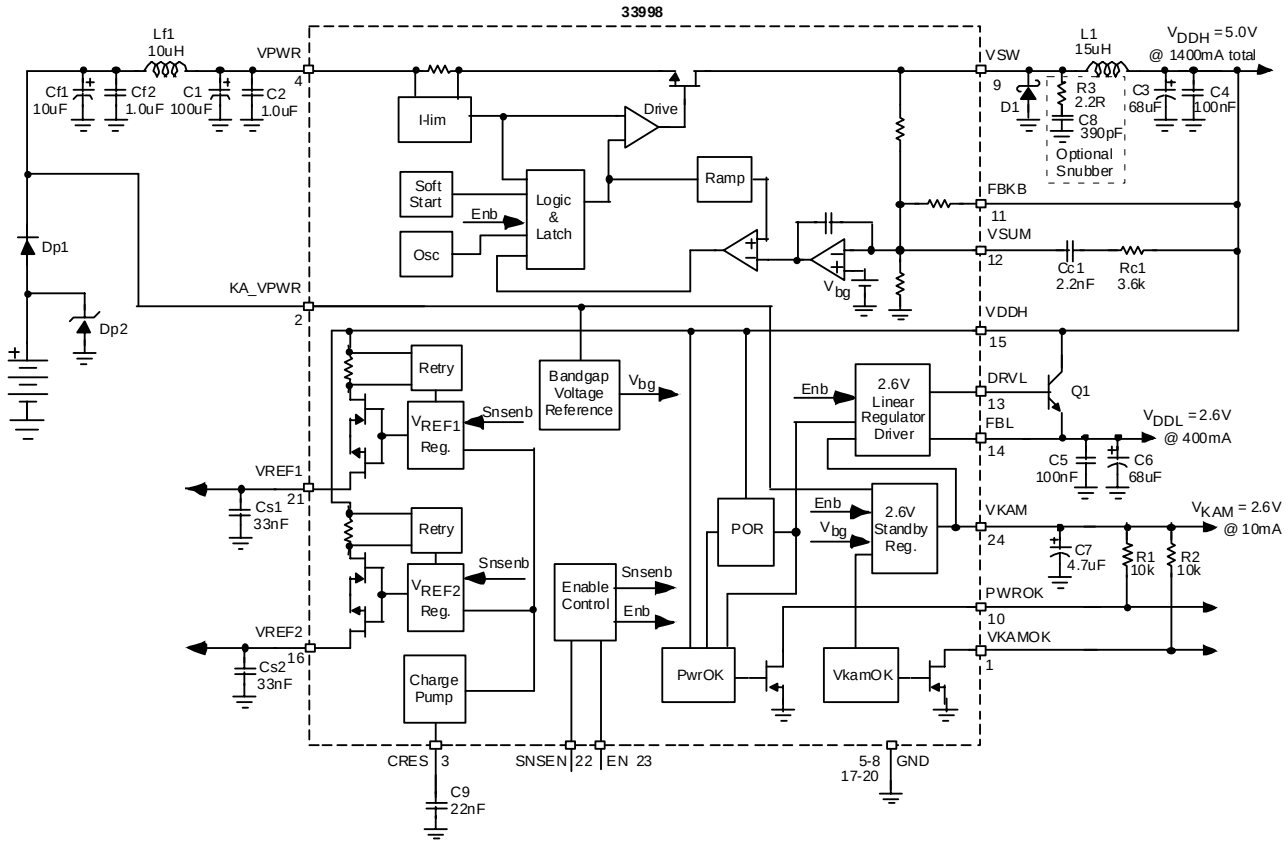
This timer starts to time out at the end of the soft-start period if the VDDH and VDDL outputs are in the valid regulation range. If the timer “times out”, then the open-drain PWROK signal is released, indicating that “power is ON”.

SUPERVISORY CIRCUITS (PWROK) AND (VKAMOK)

The 33998 has two voltage monitoring open-drain outputs, the PWROK and the VKAMOK pins. PWROK is "active high". This output is pulled low when either of the regulator outputs (VDDH or VDDL) are below their regulation windows. If both regulator outputs are above their respective lower thresholds, and the Power-On Reset Timer has expired, the output driver is turned off and this pin is at high-impedance state (see Figure 6).

The VKAMOK signal indicates a severe fault condition on the keep-alive regulator output VKAM. The VKAM output voltage is compared to the internal bandgap reference voltage. When the VKAM falls below the bandgap reference voltage level, the VKAMOK signal is pulled low.

TYPICAL APPLICATIONS



Note The VDDH total output current is 1.4 A. This includes the current used by the linear regulator VDDL and buffered outputs VREF1 and VREF2.

Figure 10. 33998 Application Circuit Schematic Diagram

Table 5. Recommended Components

Designator	Value/Rating	Description/Part No.	Manufacturer (16)
Cf1	10 µF/50 V	Aluminum Electrolytic/UUB1H100MNR	Nichicon
Cf2, C2	1.0 µF/50 V	Ceramic X7R/C1812C105K5RACTR	Kemet
C1	100 µF/50 V	Aluminum Electrolytic/UUH1V101MNR	Nichicon
C3 (15)	68 µF/10 V	Tantalum/T494D686M010AS	Kemet
C6	68 µF/10 V	Tantalum/T494D686M010AS	Kemet
C7	4.7 µF/10 V	Tantalum/T494A475M010AS	Kemet
C4, C5	100 nF/16 V	Ceramic X7R	Any Manufacturer
C8 (Optional)	390 pF/50 V	Ceramic X7R	Any Manufacturer
C9	22 nF/25 V	Ceramic X7R	Any Manufacturer
Cs1, Cs2	33 nF/25 V	Ceramic X7R	Any Manufacturer
Cc1	2.2 nF/16 V	Ceramic X7R	Any Manufacturer
R1, R2	10 kΩ	Resistor 0805, 5%	Any Manufacturer
R3 (Optional)	2.2 Ω	Resistor 0805, 5%	Any Manufacturer
Rc1	3.6 kΩ	Resistor 0805, 5%	Any Manufacturer
Lf1	10 µH	CDRH127-100M or SLF10145-100M2R5	Sumida TDK
L1	15 µH	CDRH127-150MC or SLF10145-150M2R2	Sumida TDK
Q1	1.0 A/20 V	Bipolar Transistor/BCP68T1	ON Semiconductor
D1	2.0 A/50 V	Schottky Diode/SS25	General Semiconductor
Dp1	3.0 A/200 V	Diode/MURS320	ON Semiconductor
Dp2	27 V	Transient Voltage Suppressor/SM5A27	General Semiconductor

Notes

15. It is possible to use ceramic capacitors in the switcher output, e.g. C3 = 2 x 22 µF/6.3 V X7R ceramic. In this case the compensation resistor has to be changed to Rc1 = 200 Ω to stabilize the switching regulator operation.
16. Freescale Semiconductor does not assume liability, endorse, or warrant components from external manufacturers that are referenced in circuit drawings or tables. While Freescale Semiconductor offers component recommendations in this configuration, it is the customer's responsibility to validate their application.
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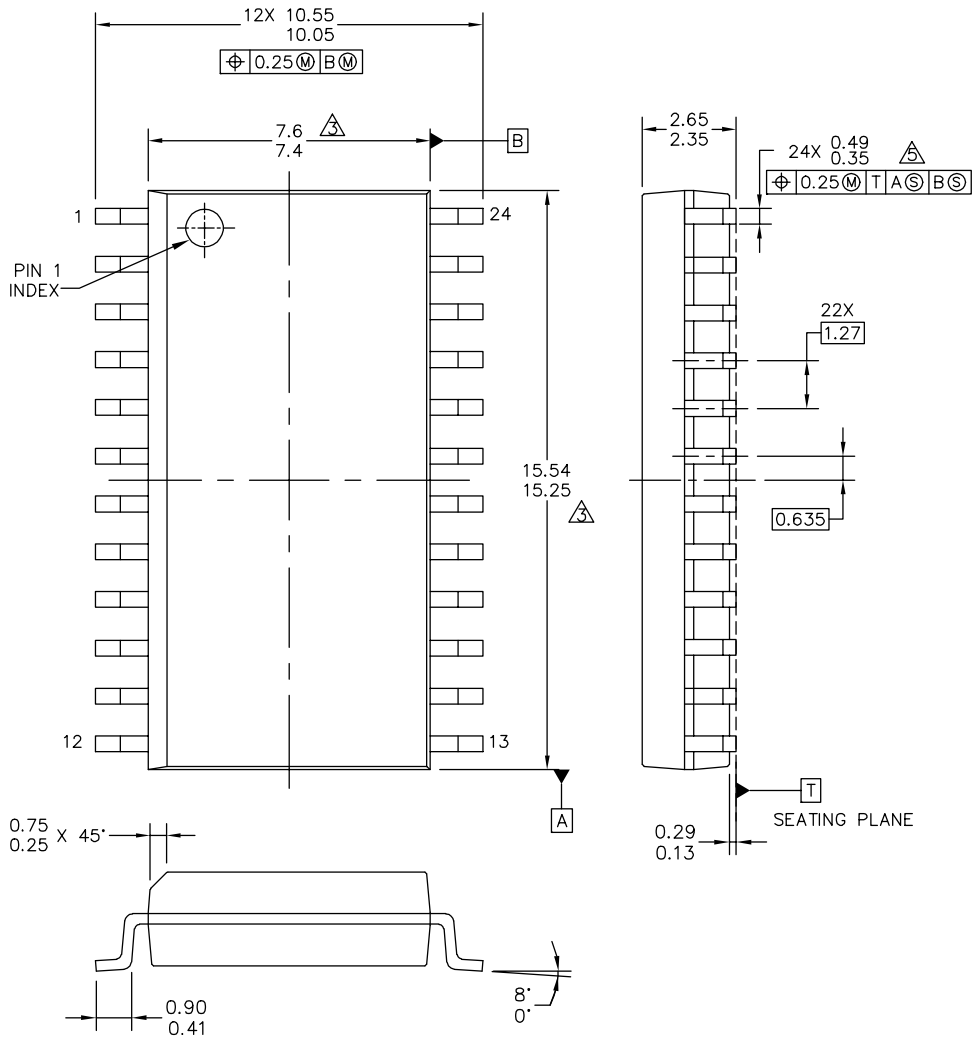
PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” listed below.



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TITLE: 24LD SOIC W/B, 1.27 PITCH 7.5 X 15.4 CASE–OUTLINE	DOCUMENT NO: 98ASB42344B	REV: F
	CASE NUMBER: 751E–04	26 APR 2005
	STANDARD: JEDEC MS–013 AD	

DWB SUFFIX
EG SUFFIX (PB-FREE)
24 PIN SOIC WIDE BODY
PLASTIC PACKAGE
98ASB42344B
ISSUE F

33998

REVISION HISTORY

Revision	Date	Description of Changes
2.0	8/2006	• Implemented Revision History page • Converted to Freescale format • Update to the prevailing form and style • Removed MC33998EG/R2, and replaced with MCZ33998EG/R2 in the Ordering Information block • Removed Peak Package Reflow Temperature During Reflow (solder reflow) parameter from Maximum Ratings on page 5. Added note with instructions from www.freescale.com.

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