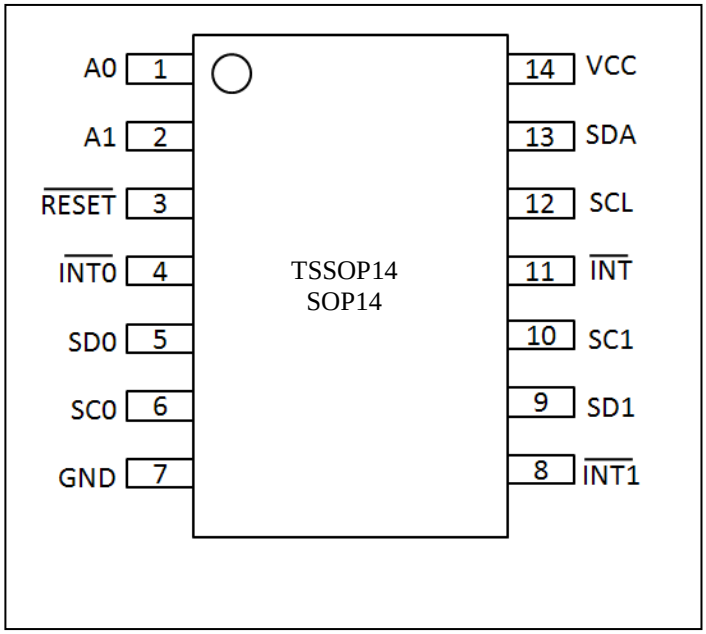
2 Channel I2C bus switch with interrupt logic and Reset

Features

- 1-of-2 bidirectional translating multiplexer
- I2C-bus interface logic
- Operating power supply voltage:1.65 V to 5.5 V
- Allows voltage level translation between 1.2V, 1.8V,2.5 V, 3.3 V and 5 V buses
- Low standby current
- Low Ron switches
- Channel selection via I2C bus
- Power-up with all multiplexer channels deselected
- Capacitance isolation when channel disabled
- No glitch on power-up
- Supports hot insertion
- 5 V tolerant inputs
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 8000 V HBM per JESD22-A114, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SOIC-14W,TSSOP-14L

Pin Configuration



Description

The PI4MSD5V9543B is a bidirectional translating switch, controlled by the I2C bus. The SCL/SDA upstream pair fans out to two downstream pairs, or channels. Any individual SCx/SDx channels or combination of channels can be selected, determined by the contents of the programmable control register. Two interrupt inputs, INT0 and INT1, one for each of the downstream pairs, are provided. One interrupt output, INT, which acts as an AND of the two interrupt inputs, is provided.

An active LOW reset input allows the PI4MSD5V9543B to recover from a situation where one of the downstream buses is stuck in a LOW state. Pulling the RESET pin LOW resets the I2C bus state machine and causes all the channels to be deselected, as does the internal power-on reset function.

The pass gates of the switches are constructed such that the VCC pin can be used to limit the maximum high voltage which will be passed by the PI4MSD5V9543X. This allows the use of different bus voltages on each SCx/SDx pair, so that 1.2V,1.8 V, 2.5 V, or 3.3 V parts can communicate with 5 V parts without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel.

All I/O pins are 5 V tolerant.

The PI4MSD5V9543A and PI4MSD5V9543B are identical except for the fixed portion of the slave address.

Pin Description

Pin No	Pin Name	Type	Description
1	A0	Input	address input 0
2	A1	Input	address input 1
3	$\overline{\text{RESET}}$	Input	active LOW reset input
4	$\overline{\text{INT0}}$	Input	active LOW interrupt input 0
5	SD0	I/O	serial data 0
6	SC0	I/O	serial clock 0
7	GND	Ground	supply ground
8	$\overline{\text{INT1}}$	Input	active LOW interrupt input 1
9	SD1	I/O	serial data 1
10	SC1	I/O	serial clock 1
11	$\overline{\text{INT}}$	Output	active LOW interrupt output
12	SCL	I/O	serial clock line
13	SDA	I/O	serial data line
14	VCC	Power	supply voltage

Block Diagram

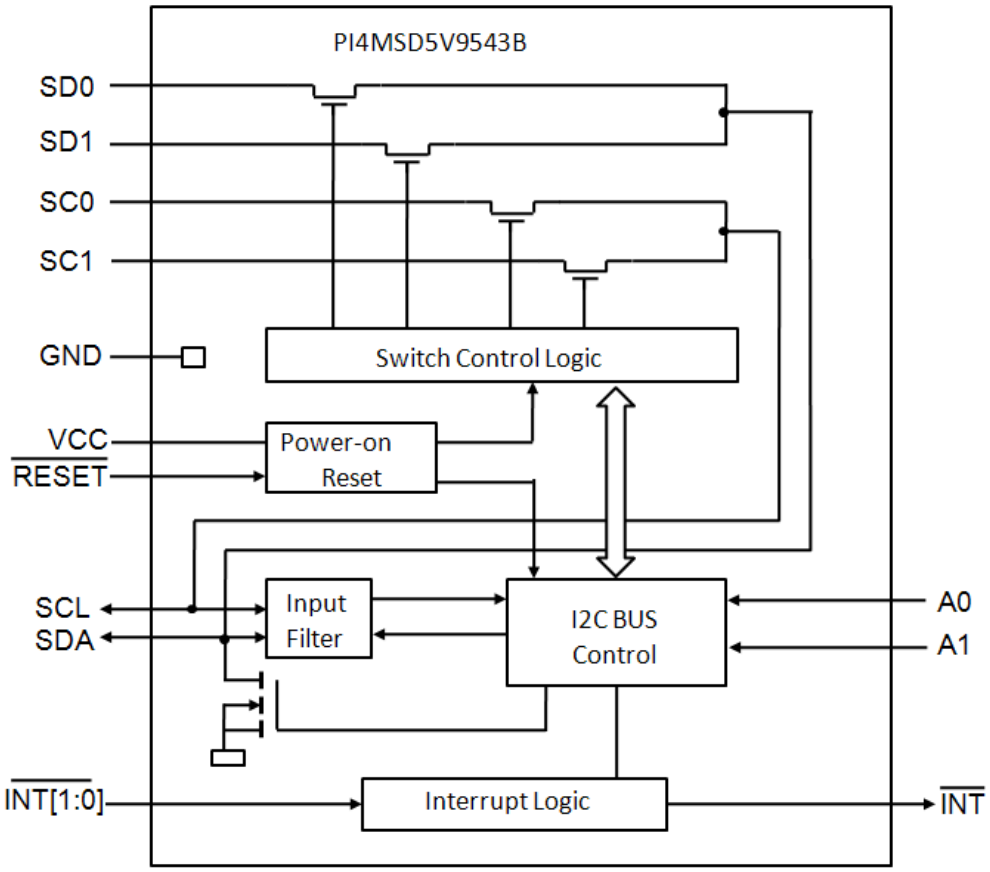


Figure 1: Block Diagram

Maximum Ratings

Storage Temperature .....–55 ℃ to +125 ℃
Supply Voltage port B .....–0.5V to +6.0V
Supply Voltage port A .....–0.5V to +6.0V
DC Input Voltage ..... –0.5V to +6.0V
Control Input Voltage (EN)… ..... –0.5V to +6.0V
Total power dissipation (1).....100mW
Input current(EN,VCCA,VCCB,GND).....50mA
ESD: HBM Mode 8000V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended operation conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	V_{CCA} Positive DC Supply Voltage	1.65	-	5.5	V
V_{EN}	Enable Control Pin Voltage	GND	-	5.5	V
V_{IO}	I/O Pin Voltage	GND	-	5.5	V
Δt /ΔV	Input transition rise or fall time	-	-	10	ns/V
T_A	Operating Temperature Range	−40	-	+85	℃

DC Electrical Characteristics

Unless otherwise specified, -40°C≤T_A≤85℃, 1.1V≤Vcc≤3.6V

Symbol	Parameter	Conditions	VCC	Min	Typ	Max	Unit
Supply							
VCC	Supply Voltage			1.65		5.5	V
ICC	supply current	operating mode; no load; V_I = VCC or GND; fSCL = 100 kHz	3.6V to 5.5V		65	100	uA
			2.3V to 3.6V		20	50	uA
			1.65V to 2.3V		10	30	uA
Istb	standby current	standby mode; VCC = 3.6 V; no load; V_I = VCC or GND; fSCL = 0 kHz	3.6V to 5.5V		0.3	1	uA
			2.3V to 3.6V		0.1	1	uA
			1.65V to 2.3V		0.1	1	uA
VPOR[1]	power-on reset voltage	no load; V_I = VCC or GND	3.6V to 5.5V		1.3	1.5	V
Input SCL; input/output SDA							
V_{IL}	LOW-level input voltage		1.65V to 5.5V	-0.5		+0.3V_{CC}	V
V_{IH}	HIGH-level input voltage		1.65V to 2V	0.75V_{CC}		6	V
			2V to 5.5V	0.7V_{CC}		6	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	1.65V to 5.5V	3		-	mA
		V_{OL} = 0.6 V	1.65V to 5.5V	6		-	mA
I_{IL}	LOW-level input current	V_I = GND	1.65V to 5.5V	-1		+1	uA
I_{IH}	HIGH-level input current	V_I = VCC	1.65V to 5.5V	-1		+1	uA
Ci	input capacitance	VI = GND	3.6V to 5.5V	-	9	10	pF
Pass Gate							
Ron	ON-state resistance	V_O = 0.4 V; I_O = 15 mA	4.5 V to 5.5 V	4	9	24	Ω
			3V to 3.6V	5	11	31	Ω
		V_O = 0.4 V; I_O = 10mA	2.3V to 2.7V	7	16	55	Ω
			1.65V to 2V	9	20	70	Ω
Vpass	switch output voltage	Vin =VCC; Iout = -100uA	5V		3.6		V
			4.5 V to 5.5 V	2.8		4.5	V
			3.3V		2.2		V
			3V to 3.6V	1.6		2.8	V
			2.5V		1.5		V
			2.3V to 2.7V	1.1		2	V
			1.8V		0.9		V
			1.65V to 2V	0.54		1.3	V
I_L	leakage current	VI = VCC or GND	1.65V to 5.5V	-1		+1	uA
Cio	input/output capacitance	VI = VCC or GND	1.65V to 5.5V		3	5	pF

To be continued

Continued

Symbol	Parameter	Conditions	VCC	Min	Typ	Max	Unit
Select inputs A0, A1, INT0, INT1							
V_{IL}	LOW-level input voltage		1.65V to 5.5V	-0.5		$+0.3V_{CC}$	V
V_{IH}	HIGH-level input voltage		1.65V to 5.5V	$0.7V_{CC}$		6	V
I_{IL}	LOW-level input current	V_I = GND	1.65V to 5.5V	-1		+1	uA
Ci	input capacitance	V_I = GND	1.65V to 5.5V		3	5	pF
INT output							
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	1.65V to 5.5V	3			mA
I_{OH}	HIGH-level output current		1.65V to 5.5V			+10	uA

Note: VCC must be lowered to 0.2 V for at least 5 us in order to reset part.

AC Electrical characteristics

Tamb = - 40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	VCC	Min	Typ	Max	Unit
t_{PD}[1]	propagation delay	from SDA to SDx, or SCL to SCx	1.65V to 5.5V			0.3	ns
INT[2]							
t_{V_INT}	valid time from INTn to INT signal		1.65V to 5.5V			4	us
t_{D_INT}	delay time from INTn to INT inactive		1.65V to 5.5V			2	us
t_{REJ_L}	LOW-level rejection time		1.65V to 5.5V	1			us
t_{REJ_H}	HIGH-level rejection time		1.65V to 5.5V	0.5			us
RESET							
tw(rst)L	LOW-level reset time			4			ns
trst	reset time	SDA clear		500			ns
$t_{REC;STA}$	recovery time to START condition			0			ns

Note
[1]Pass gate propagation delay is calculated from the 20Ω typical Ron and the 15 pF load capacitance.
[2] Measurements taken with 1 kΩpull-up resistor and 50 pF load.

I2C Interface Timing Requirements

Symbol	Parameter	STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
		MIN	MAX	MIN	MAX	
fscl	I2C clock frequency	0	100	0	400	kHz
t_{Low}	I2C clock high time	4.7		1.3		µs
t_{High}	I2C clock low time	4		0.6		µs
t_{SP}	I2C spike time		50		50	ns
$t_{SU:DAT}$	I2C serial-data setup time	250		100		ns
$t_{HD:DAT}$	I2C serial-data hold time	0 [1]		0 [1]		µs
tr	I2C input rise time		1000		300	ns
tf	I2C input fall time		300		300	ns
t_{BUF}	I2C bus free time between stop and start	4.7		1.3		µs
$t_{SU:STA}$	I2C start or repeated start condition setup	4.7		0.6		µs
$t_{HD:STA}$	I2C start or repeated start condition hold	4		0.6		µs
$t_{SU:STO}$	I2C stop condition setup	4		0.6		µs
$t_{VD:DAT}$	Valid-data time (high to low) [2] SCL low to SDA output low valid		1		1	µs
	Valid-data time (low to high) [2] SCL low to SDA output high valid		0.6		0.6	µs
$t_{VD:ACK}$	Valid-data time of ACK condition ACK signal from SCL low to SDA output low		1		1	µs
Cb	I2C bus capacitive load		400		400	pF

Notes:
[1] A device internally must provide a hold time of at least 300 ns for the SDA signal (referred to as the VIH min of the SCL signal), in order to bridge the undefined region of the falling edge of SCL.
[2] Data taken using a 1-kΩ pull up resistor and 50-pF load Notes

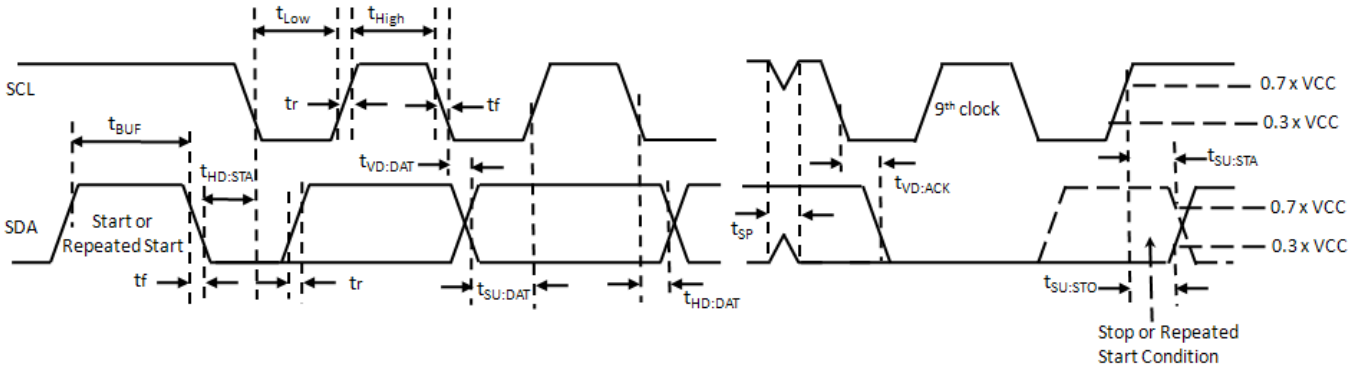


Figure 2. Definition of timing on the I2C-bus

Application

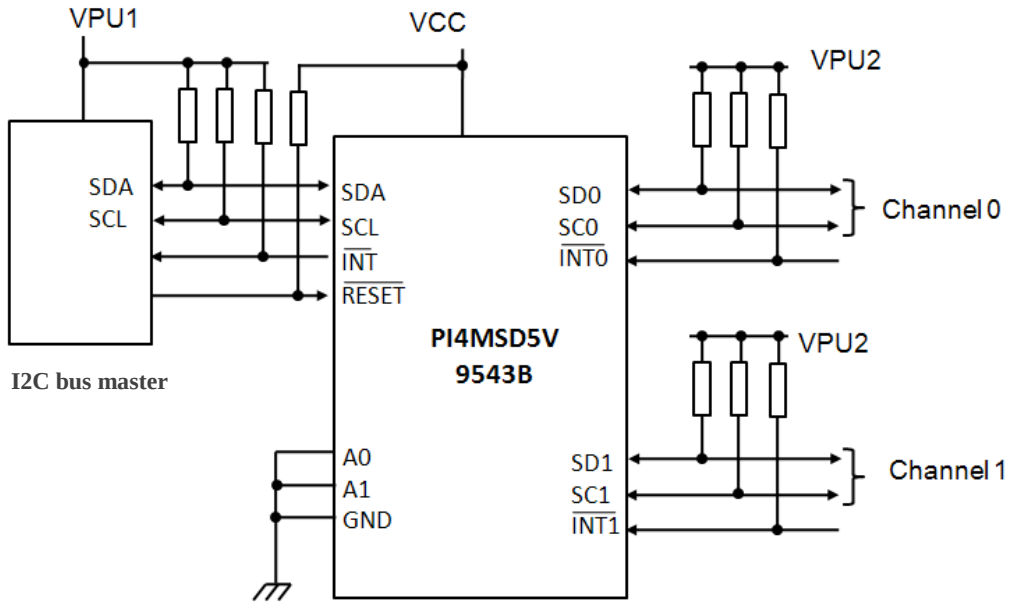


Figure 3. Typical Application

VCC	VPU1	VPU2
1.8V	1.5V-5.5V	1.2V-5.5V
2.5V	1.8V-5.5V	1.8V-5.5V
3.3V	2.7V-5.5V	2.7V-5.5V
5V	4.5V-5.5V	4.5V-5.5V

Note:
If the device generating the interrupt has an open-drain output structure or can be 3-stated, a pull-up resistor is required.
If the device generating the interrupt has a totem pole output structure and cannot be 3-stated, a pull-up resistor is not required.
The interrupt inputs should not be left floating.

Device addressing

Following a START condition the bus master must output the address of the slave it is accessing. The address of the PI4MSD5V9543B is shown in Figure 4.

To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

The last bit of the slave address defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

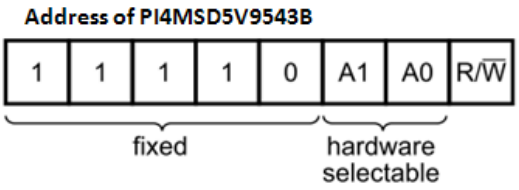


Figure 4:Device address

The PI4MSD5V9543B is an alternate address version, if needed for larger systems or to resolve address conflicts. The data sheet will reference the PI4MSD5V9543A, but the PI4MSD5V9543B functions identically except for the slave address.

Control register

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PI4MSD5V9543B, which will be stored in the control register. If multiple bytes are received by the PI4MSD5V9543B, it will save the last byte received. This register can be written and read via the I2C-bus.

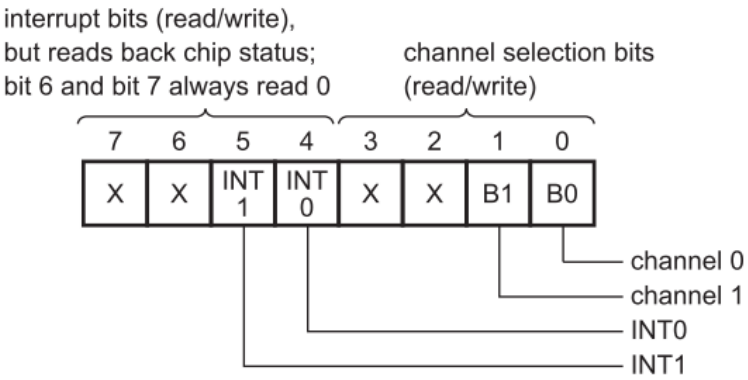


Figure 5: Control register

Control register definition

One or several SCx/SDx downstream pair, or channel, is selected by the contents of the control register. This register is written after the PI4MSD5V9543B has been addressed. The 2 LSBs of the control byte are used to determine which channel is to be selected. When a channel is selected, the channel will become active after a STOP condition has been placed on the I2C-bus. This ensures that all SCx/SDx lines will be in a HIGH state when the channel is made active, so that no false conditions are generated at the time of connection.

Bits INT0, INT1, D6 and D7 are all writable, but will read the chip status. INT0 and INT1 indicate the state of the corresponding interrupt input. D7 and D6 always read 0.

D7	D6	INT1	INT0	D3	B2	B1	B0	Command
X	X	X	X	X	X	X	0	channel 0 disabled
							1	channel 0 enabled
X	X	X	X	X	X	0	X	channel 1 disabled
						1		channel 1enabled
0	0	0	0	0	0	0	0	no channel selected; power-up/reset default state

Control register: Write—channel selection; Read—channel status.

Remark: Channel 0 and channel 1 can be enabled at the same time. Care should be taken not to exceed the maximum bus capacitance.

Interrupt handling

The PI4MSD5V9543B provides 2 interrupt inputs, one for each channel, and one open-drain interrupt output. When an interrupt is generated by any device, it will be detected by the PI4MSD5V9543B and the interrupt output will be driven LOW. The channel need not be active for detection of the interrupt. A bit is also set in the control register.

Bit 4 and bit 5 of the control register corresponds to the INT0 and INT1 inputs of the PI4MSD5V9543B, respectively. Therefore, if an interrupt is generated by any device connected to channel 1, the state of the interrupt inputs is loaded into the control register when a read is accomplished. Likewise, an interrupt on any device connected to channel 0 would cause bit 4 of the control register to be set on the read. The master can then address the PI4MSD5V9543B and read the contents of the control register to determine which channel contains the device generating the interrupt. The master can then reconfigure the PI4MSD5V9543B to select this channel, and locate the device generating the interrupt and clear it.

It should be noted that more than one device can provide an interrupt on a channel, so it is up to the master to ensure that all devices on a channel are interrogated for an interrupt.The interrupt inputs may be used as general-purpose inputs if the interrupt function is not required.

If unused, interrupt inputs must be connected to VCC through a pull-up resistor.

D7	D6	INT1	INT0	D3	D2	B1	B0	Command
0	0	X	0	X	X	X	X	no interrupt on channel 0
			1					interrupt on channel 0
0	0	0	X	X	X	X	X	no interrupt on channel 1
		1						interrupt on channel 1

Control register read — interrupt

The Reset Pin

The RESET input is an active LOW signal which may be used to recover from a bus fault condition. By asserting this signal LOW for a minimum of tw(rst)L, the PI4MSD5V9543B will reset its registers and I2C-bus state machine and will deselect all channels. The RESET input must be connected to VCC through a pull-up resistor.

Power-on reset

When power is applied to VCC, an internal Power-On Reset (POR) holds the PI4MSD5V9543B in a reset condition until VCC has reached VPOR. At this point, the reset condition is released and the PI4MSD5V9543B registers and I2C-bus state machine are initialized to their default states (all zeroes), causing all the channels to be deselected. Thereafter, VCC must be lowered below 0.2 V for at least 5 us in order to reset the device.

Voltage translation

The pass gate transistors of the PI4MSD5V9543B are constructed such that the VCC voltage can be used to limit the maximum voltage that is passed from one I2C-bus to another.

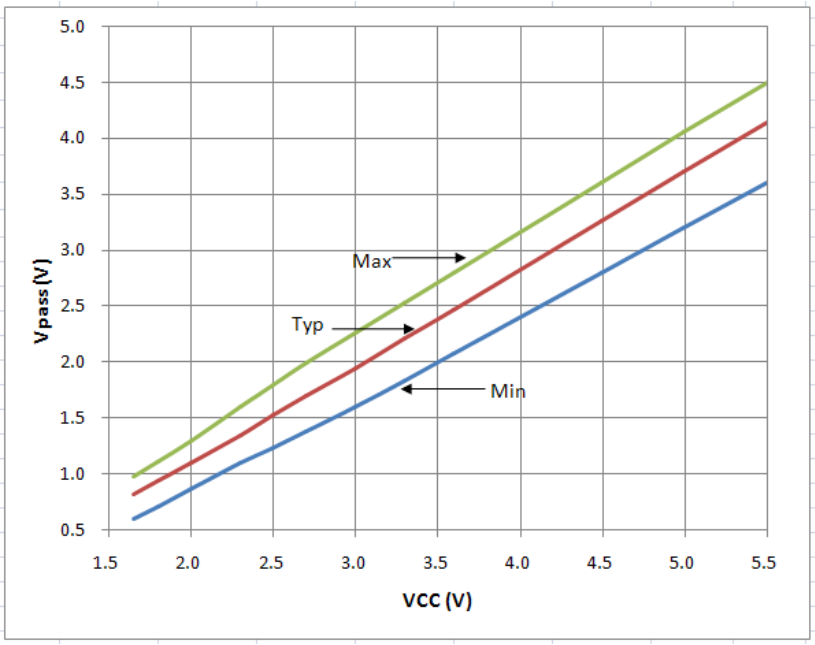


Figure 6:Vpass voltage VS Vcc

Figure 6 shows the voltage characteristics of the pass gate transistors (note that the graph was generated using the data specified in Section "DC Electrical characteristics" of this data sheet).

In order for the PI4MSD5V9543B to act as a voltage translator, the Vpass voltage should be equal to, or lower than the lowest bus voltage. For example, if the main bus was running at 5 V, and the downstream buses were 3.3 V and 2.7 V, then Vpass should be equal to or below 2.7 V to clamp the downstream bus voltages effectively.

Looking at Figure 6, we see that Vpass (max) is at 2.7 V when the PI4MSD5V9543B supply voltage is 3.5 V or lower so the PI4MSD5V9543B supply voltage could be set to 3.3 V. Pull-up resistors can then be used to bring the bus voltages to their appropriate levels

I2C BUS

The I2C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time are interpreted as control signals

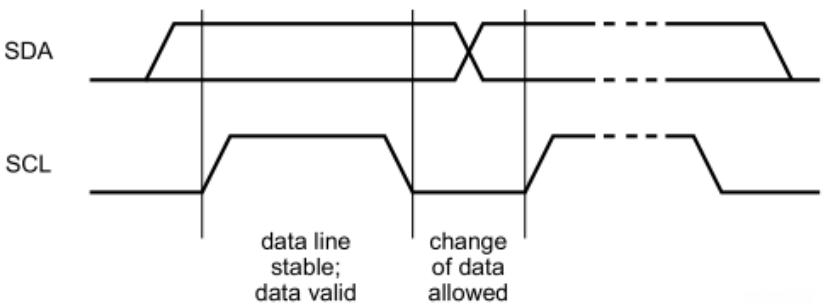


Figure 7: Bit Transfer

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P)

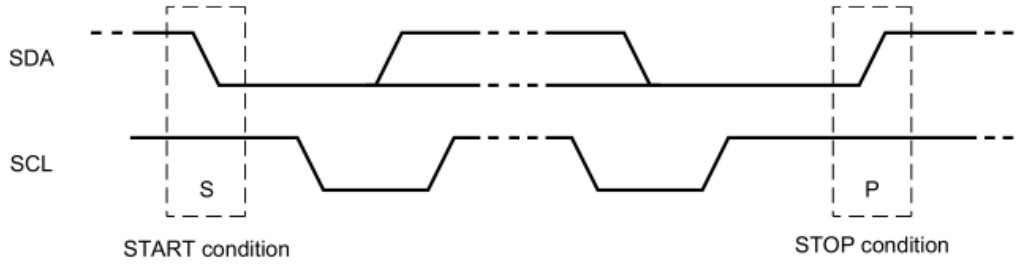


Figure 8. Definition of Start and Stop Conditions

A device generating a message is a ‘transmitter’, a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’

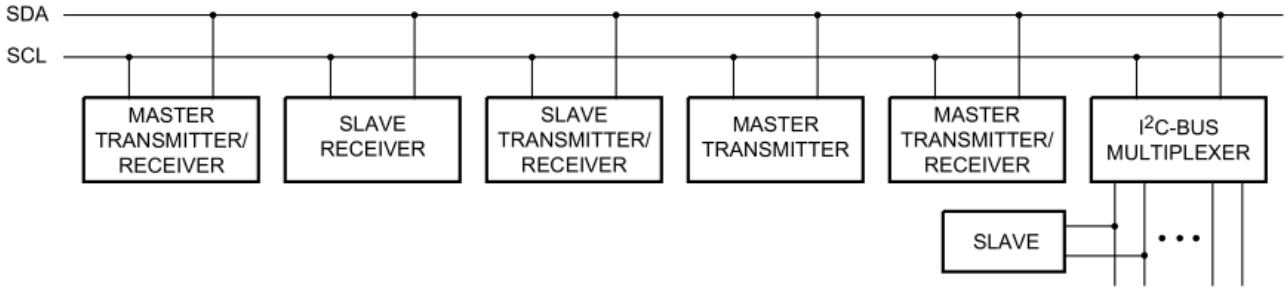


Figure 9. System Configuration

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of 8 bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also, a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

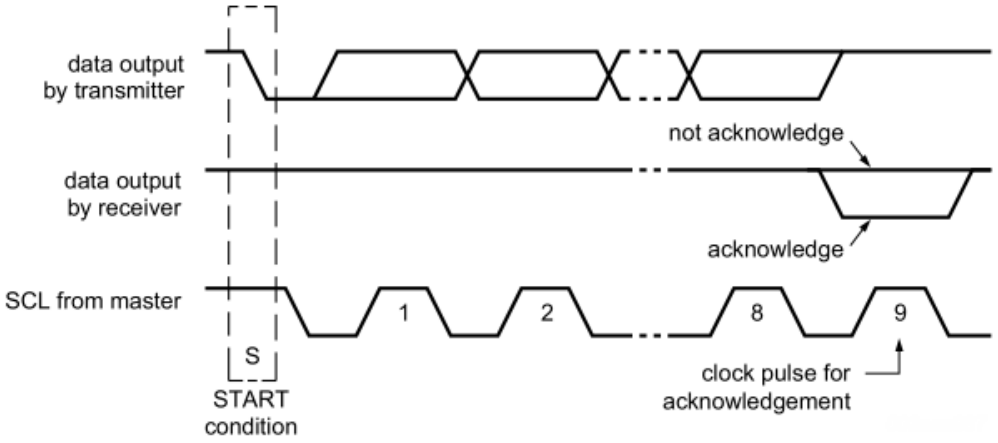


Figure 10. Acknowledgment on I2C Bus

Data is transmitted to the PI4MSD5V9543B control register using the write mode shown in bellow

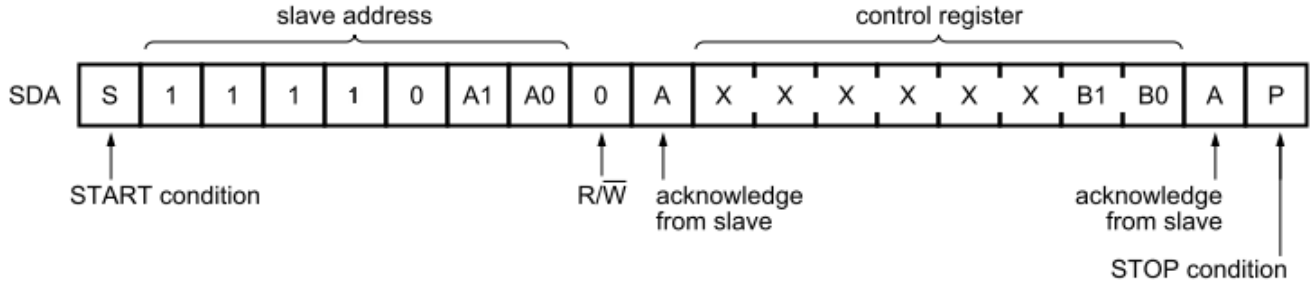


Figure 11. Write Control Register

Data is transmitted to the PI4MSD5V9543B control register using the write mode shown in bellow

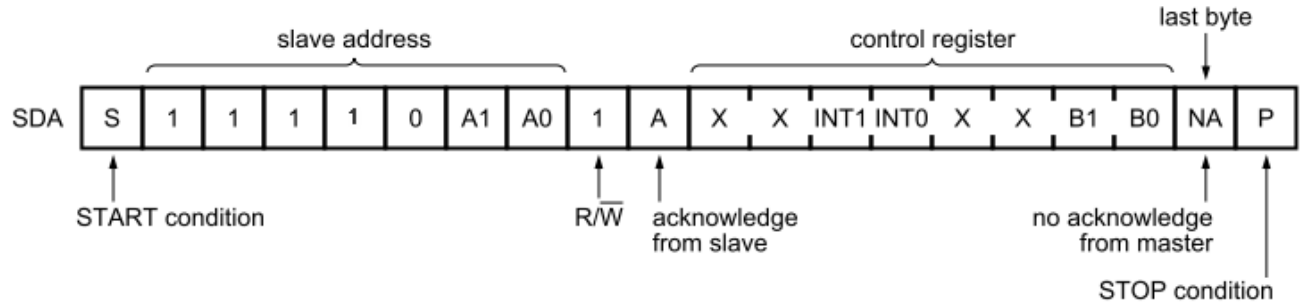
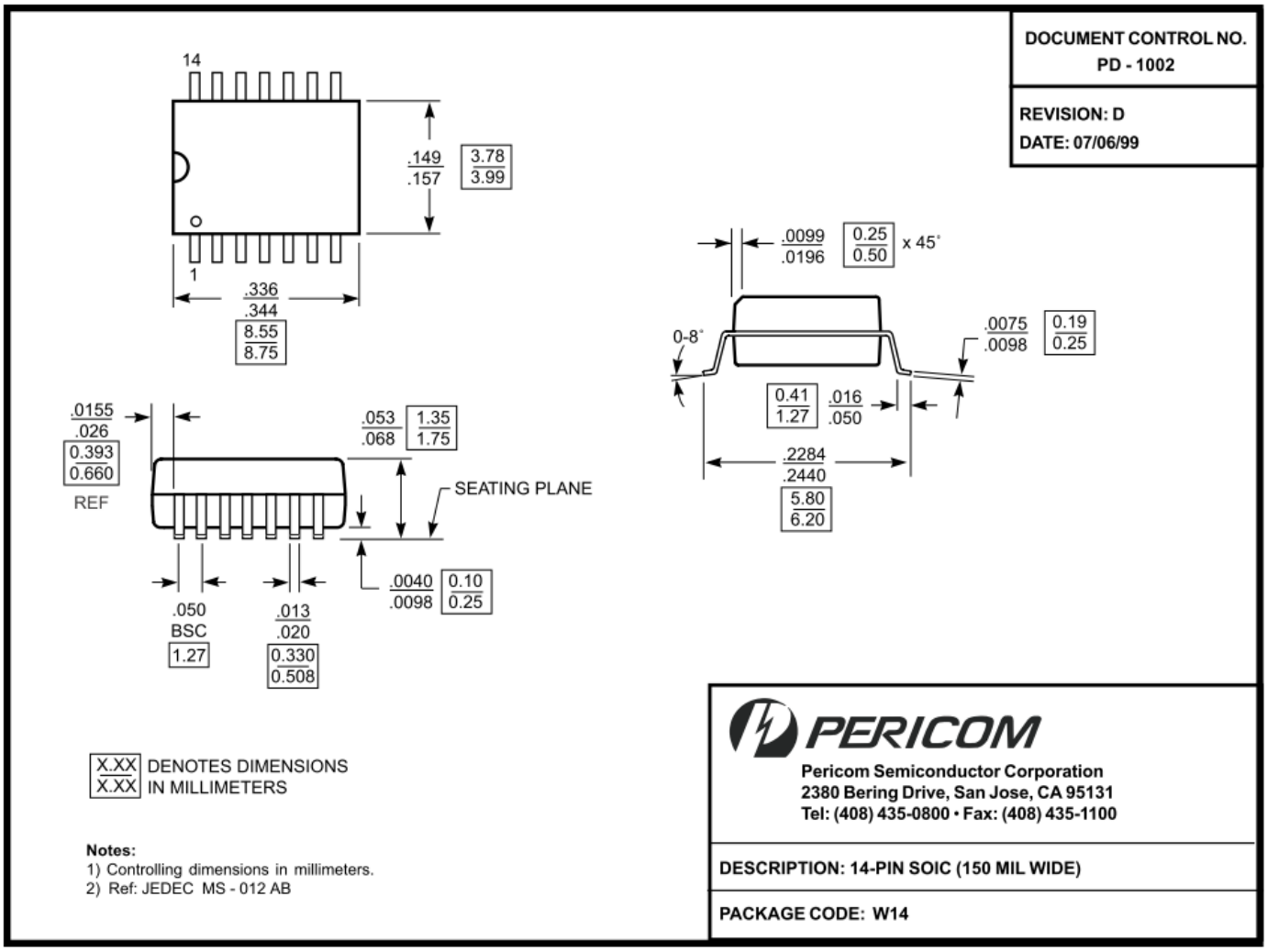


Figure 12. Read Control Register

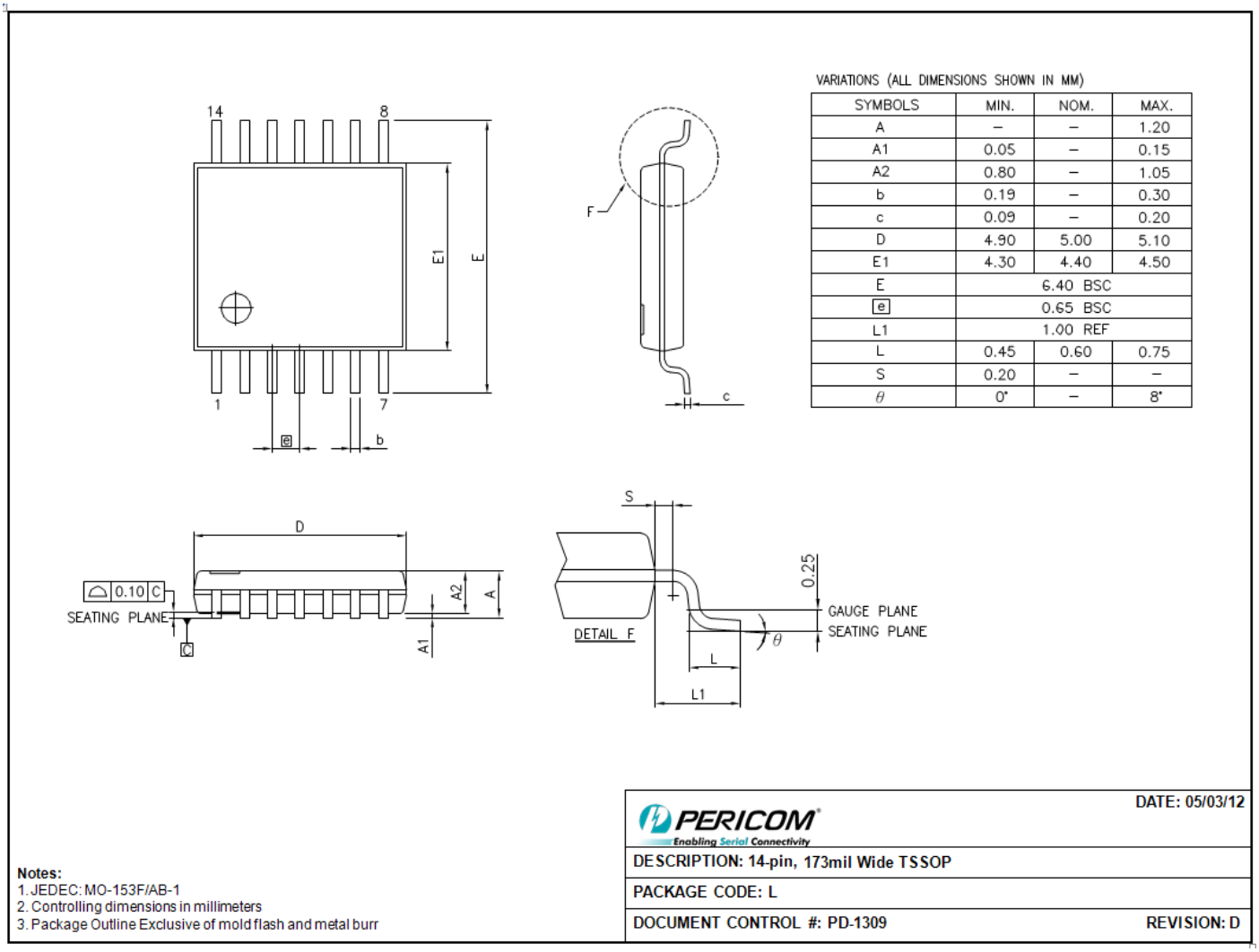
Mechanical Information

SOIC-14(W)



Mechanical Information

TSSOP-14(L)



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	–	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

Notes:
1. JEDEC: MO-153F/AB-1
2. Controlling dimensions in millimeters
3. Package Outline Exclusive of mold flash and metal burr

PERICOM Enabling Serial Connectivity

DATE: 05/03/12

DESCRIPTION: 14-pin, 173mil Wide TSSOP

PACKAGE CODE: L

DOCUMENT CONTROL #: PD-1309 REVISION: D

Ordering Information

Part No.	Package Code	Package
PI4MSD5V9543BWE	W	14-Pin,150 mil Wide SOIC
PI4MSD5V9543BWEX	W	14-Pin,150 mil Wide SOIC, Tape & Reel
PI4MSD5V9543BLE	L	14-Pin,173 mil Wide TSSOP
PI4MSD5V9543BLEX	L	14-Pin,173 mil Wide TSSOP, Tape & Reel

Note:
- E = Pb-free and Green
- Adding X Suffix= Tape/Reel