TMD2725

ALS, and Small Aperture Proximity Sensor Module

General Description

The device features advanced proximity measurement and digital ambient light sensing (ALS). The package has been designed to accommodate a single small aperture approach. The slim module incorporates an IR LED and factory calibrated LED driver. The proximity detection feature provides object detection (e.g. mobile device screen to user's ear) by photodiode detection of reflected IR energy (sourced by the integrated LED). Detect/release events are interrupt driven, and occur when proximity result crosses upper and/or lower threshold settings. The proximity engine features offset adjustment registers to compensate for unwanted IR energy reflection at the sensor. Proximity results are further improved by automatic ambient light subtraction. The ALS detection feature provides photopic light intensity data. The ALS photodiode has UV and IR blocking filters and a dedicated data converter producing 16-bit data. This architecture allows applications to accurately measure ambient light which enables devices to calculate illuminance to control display backlight.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of TMD2725, ALS, and Small Aperture Proximity Sensor Module are listed below:

Figure 1:
Added Value of Using TMD2725

Benefits	Features
• Small aperture requirements	• 1.055mm emitter to detector distance
• Single device integrated optical solution	• ALS + proximity • 2mm x 3.65mm x 1mm • Integrated IR LED • Power management features • I^2C fast mode interface compatible
• Accurate ambient light sensing	• Photopic Ambient Light Sensor (ALS) • UV / IR blocking filters • Programmable gain and integration time
• Reduced power consumption	• 1.8V power supply with 1.8V I^2C bus

Applications

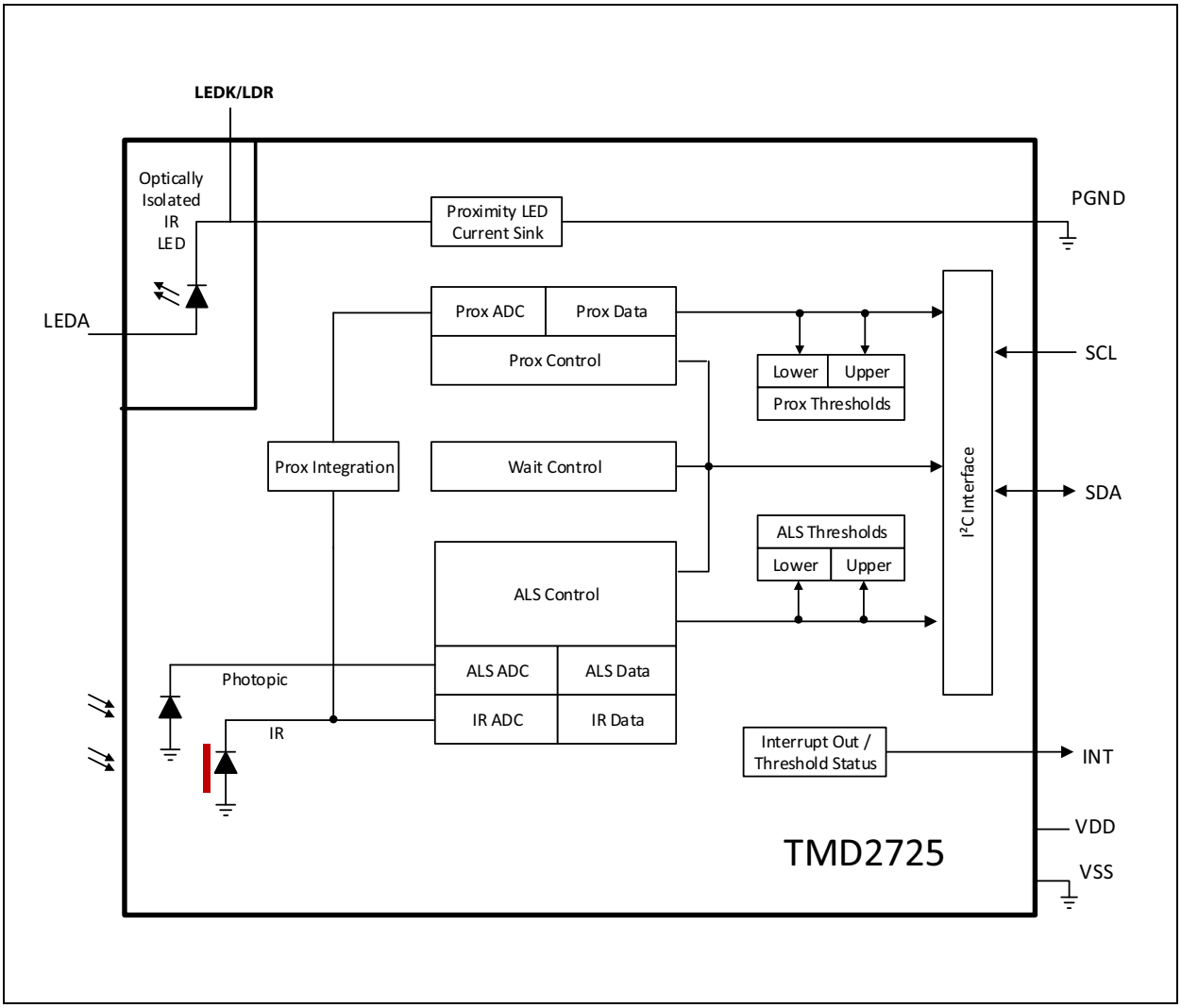
The TMD2725 applications include:

- Ambient light sensing
- Single hole proximity sensing
- Mobile phone touch screen disable

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
Functional Blocks of TMD2725



Pin Assignments

Figure 3:
Pin Diagram of TMD2725

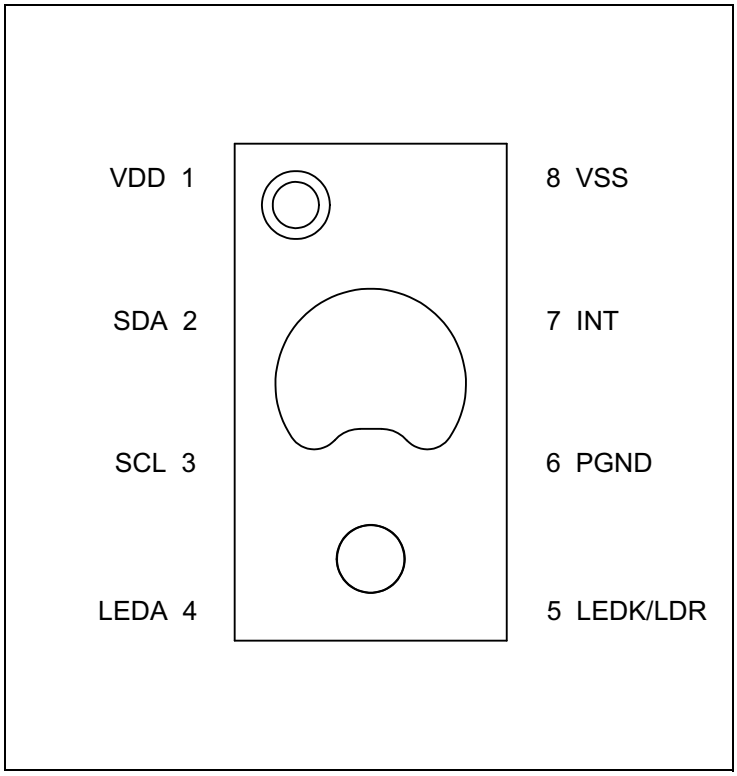


Figure 4:
Pin Description of TMD2725 (8-Pin Module)

Pin Number	Pin Name	Description
1	VDD	Supply voltage
2	SDA	I^2C serial data I/O terminal
3	SCL	I^2C serial clock input terminal
4	LEDA	LED anode
5	LEDK/LDR	This test point is the junction of the LED cathode and internal current source. Do not connect.
6	PGND	Ground for LED current sink and digital core
7	INT	Interrupt. Open drain output (active low)
8	VSS	Ground. All voltages are referenced to GND

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
VDD	Supply Voltage to Ground	-0.3	2.2	V	
LEDA	LED Voltage to PGND	-0.3	3.6	V	
V_{IO}	Digital I/O terminal voltage	-0.3	3.6	V	
I_{IO}	SDA, INT Output terminal current	-1	20	mA	
Electrostatic Discharge					
I_{SCR}	Input Current (latch up immunity) JEDEC JESD78D	± 100		mA	Class II
ESD_{HBM}	Electrostatic Discharge HBM JS-001-2014	± 2000		V	
ESD_{CDM}	Electrostatic Discharge CDM JEDEC JESD22-C101F	± 500		V	
Temperature Ranges and Storage Conditions					
T_A	Operating Ambient Temperature	-30	85	°C	
T_{STRG}	Storage Temperature Range	-40	85	°C	
T_{BODY}	Package Body Temperature		260	°C	IPC/JEDEC J-STD-020 The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices."
RH_{NC}	Relative Humidity (non-condensing)	5	85	%	
MSL	Moisture Sensitivity Level	3			Maximum floor life time 168 hours

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Electrical Characteristics of TMD2725

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC}	Oscillator frequency			8.0		MHz
IDD	Supply Current (1)	Active ALS State (PON=AEN=1, PEN=0) (2)		80	150	µA
		Idle State (PON=1,AEN=PEN=0) (3)		30	60	
		Sleep State (4)		0.7	5	
VOL	INT, SDA output low voltage	6mA sink current			0.6	V
ILEAK	Leakage current, SDA,SCL,INT		-5		5	µA
VIH	SCL, SDA input high voltage (5)		1.26			V
VIL	SCL, SDA input low voltage				0.54	V
T_{Active}	Time from power-on to ready to receive I^2C commands			1.5		ms

Note(s):

1. Values are shown at the VDD pin and do not include current through the IR LED.
2. This parameter indicates the supply current during periods of ALS integration. If Wait is enabled (WEN=1), the supply current is lower during the Wait period.
3. Idle state occurs when PON=1 and all functions are not enabled.
4. Sleep state occurs when PON = 0 and I^2C bus is idle. If Sleep state has been entered as the result of operational flow, SAI = 1, PON will remain high.
5. Digital pins: SDA, SCL, INT, are tolerant to a communication voltage up to 3.0V

Figure 7:
Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
V_{DD} supply range	1.7	1.8	2.0	V
V_{LEDA} supply voltage range (1)	3.0	3.3	3.6	V
Voltage on pin with respect to ground; SDA, SCL, INT	-0.3		3.6	V

Note(s):

1. While the device is operational across the temperature range, performance will vary with temperature. Operational characteristics are at 25°C, unless otherwise noted.

Figure 8:
Proximity Optical Characteristics of TMD2725

Parameter	Conditions	Min	Typ	Max	Unit
Part to part variation (1)	Conditions: PGAIN = 2 (4x) PLDRIVE = 8 (54mA) PPULSE = 15 (16 pulses) PPULSE_LEN = 1 (8µs) d=23mm round target 30mm target distance	75	100	125	%
Response, absolute	Basic proximity measurement (2) Conditions: PGAIN = 2 (4x), PLDRIVE = 16 (102mA) PPULSE = 15 (16 pulses) PPULSE_LEN = 2 (16µs) Target material: 90% reflective surface of Kodak gray card Target Size: 100mm x 100mm Target Distance: 100mm	128	160	192	Counts
Response, no target	PGAIN = 2 (4x) ILEDDRIVE = 16 (102mA) PPULSE = 16 (17 Pulses) Pulse Length = 2 (16µS)	0		20	
Noise/Signal (3)	PGAIN = 2 (4x) IRLEDDRIVE = 8 (54mA) PPULSE = 15 (16 pulses) PPULSE_LEN = 1 (8µs) d=23mm round target 30mm target distance			1.2	%

Note(s):

1. Production tested result is the average of 5 readings expressed relative to a calibrated response.
2. Representative result by characterization.
3. Production tested result is the average of 20 readings divided by the maximum proximity value 255.

Figure 9:
Optical Characteristics of TMD2725

Parameter	Conditions	Clear Channel			Unit
		Min	Typ	Max	
Re Irradiance responsivity Settings: AGAIN = 16x ATIME = 400ms	λ_D = 465 nm LED, 53.8 µW/cm^2		58		Count/ (µW/cm^2)
	λ_D = 530 nm LED, 43.9 µW/cm^2		490		
	λ_D = 620 nm LED, 37.5 µW/cm^2		405		
	Warm White LED, 45.6 µW/cm^2		363		
	Warm White LED, 45.6 µW/cm^2	14025	16500	18975	Counts
	λ_D = 950 nm LED, 21.1 µW/cm^2		8		Count/ (µW/cm^2)

Figure 10:
ALS Optical Characteristics of TMD2725

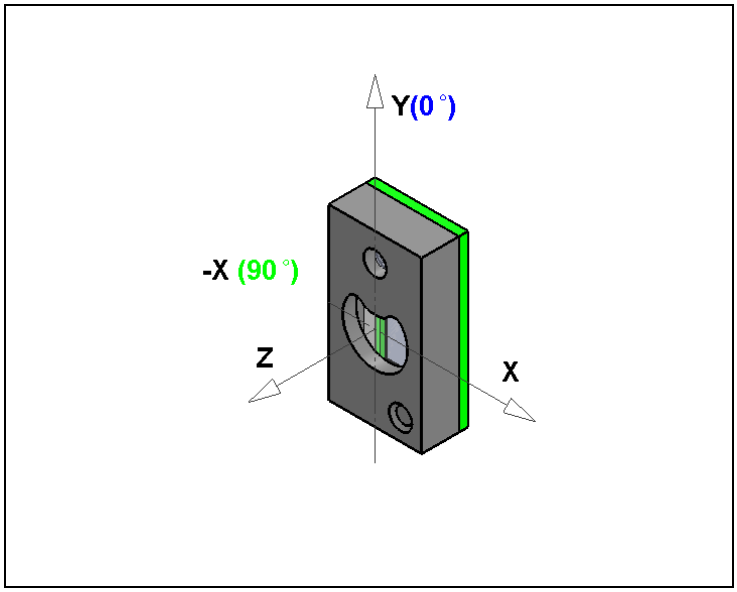
Parameter	Conditions	Min	Typ	Max	Unit
Integration time step size		2.72	2.82	2.94	ms
Dark ADC count value	Ee = 0 µW/ cm^2 AGAIN: 64x ATIME = 100ms (0xDC)	0	1	3	Counts
Gain Scaling, relative to 1x gain setting Settings: Irradiance = 17.26uW ATIME = 400ms Distance = ~33cm	AGAIN = 1x		1		x
	AGAIN = 4x		4.034		
	AGAIN = 16x		15.93		
	AGAIN = 64x		65.93		
ADC noise	AGAIN = 16x		0.005		% full scale
Lux accuracy (1)	White LED, 2700k	90	100	110	%

Note(s):

1. Not production tested. Representative result by laboratory characterization.

Typical Operating Characteristics

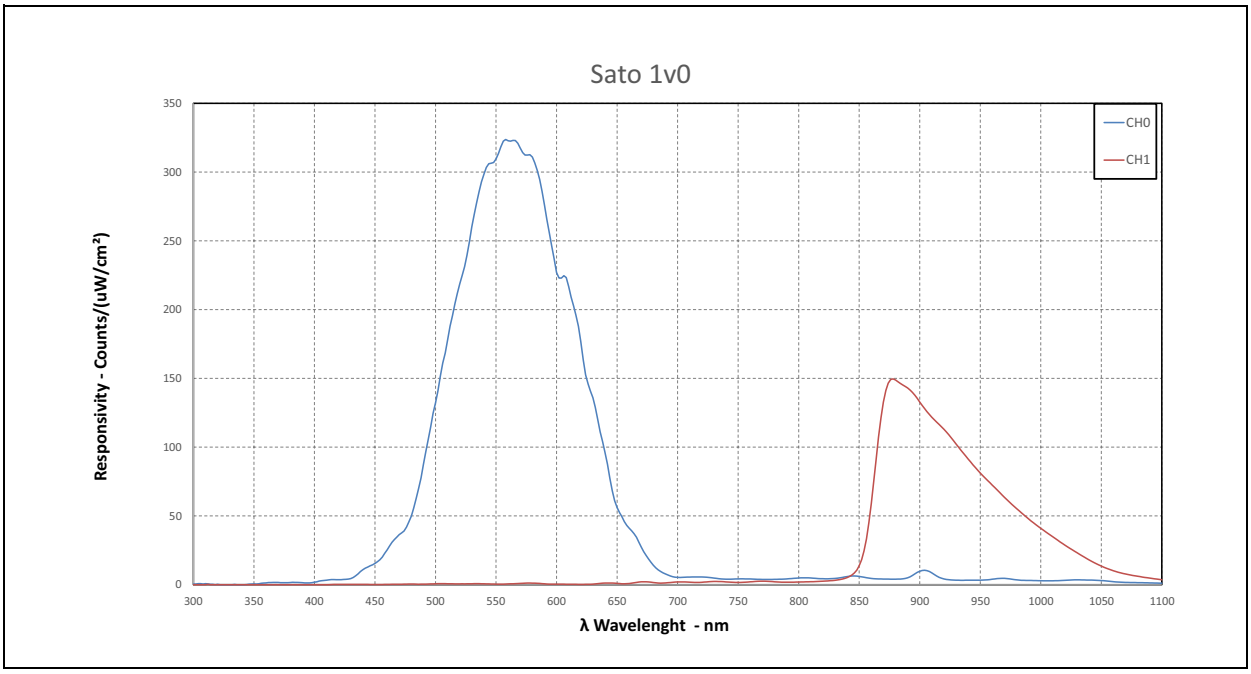
Figure 11:
Diagram Showing the YZ and XZ Planes



Note(s):

1. YZ plane (0°) represents vertical angular distribution plot (-90° to 90°)
2. XZ plane (90°) represents horizontal angular distribution plot (-90° to 90°)

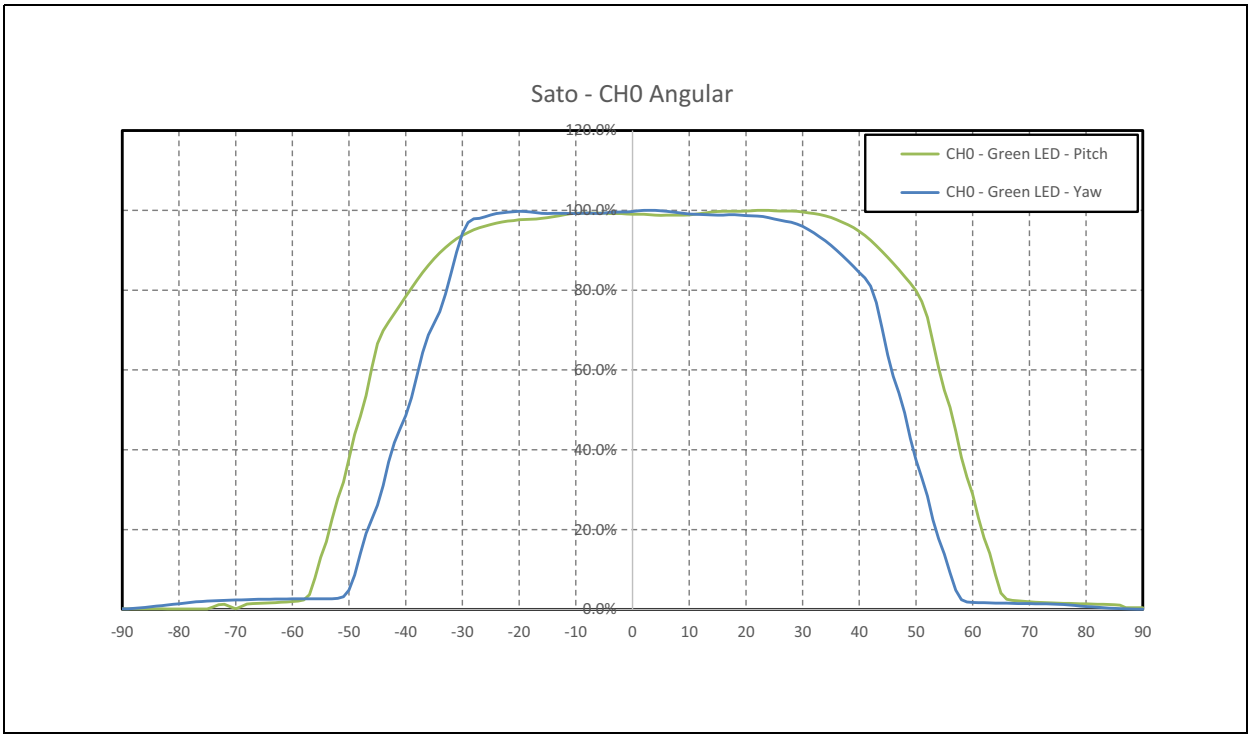
Figure 12:
Typical Spectral Response of TMD2725



Note(s):

1. Test Conditions: Gain = 16x, ATIME = 180ms
2. CH0 = ALS, CH1 = Proximity

Figure 13:
Typical ALS Angular Response



Note(s):

1. Pitch = X/Z Plane
2. Yaw = Y/Z Plane

Figure 14:
ALS Linearity

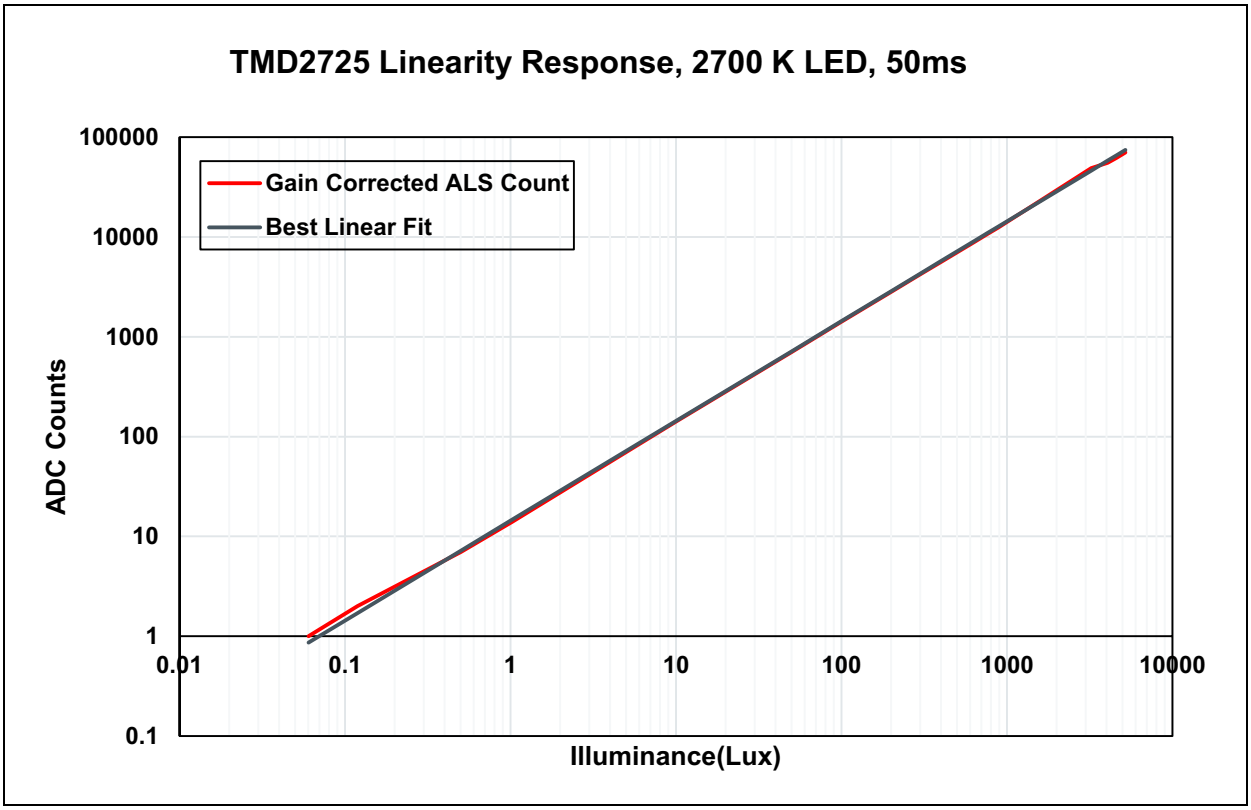
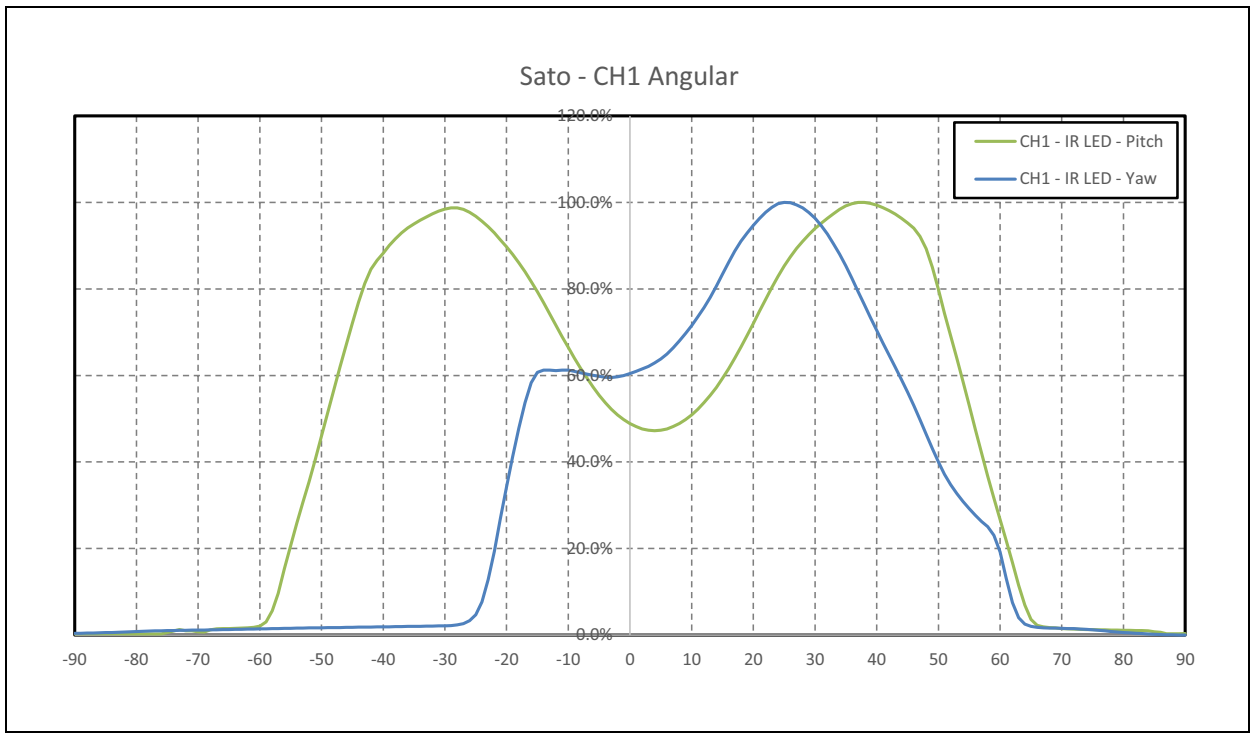


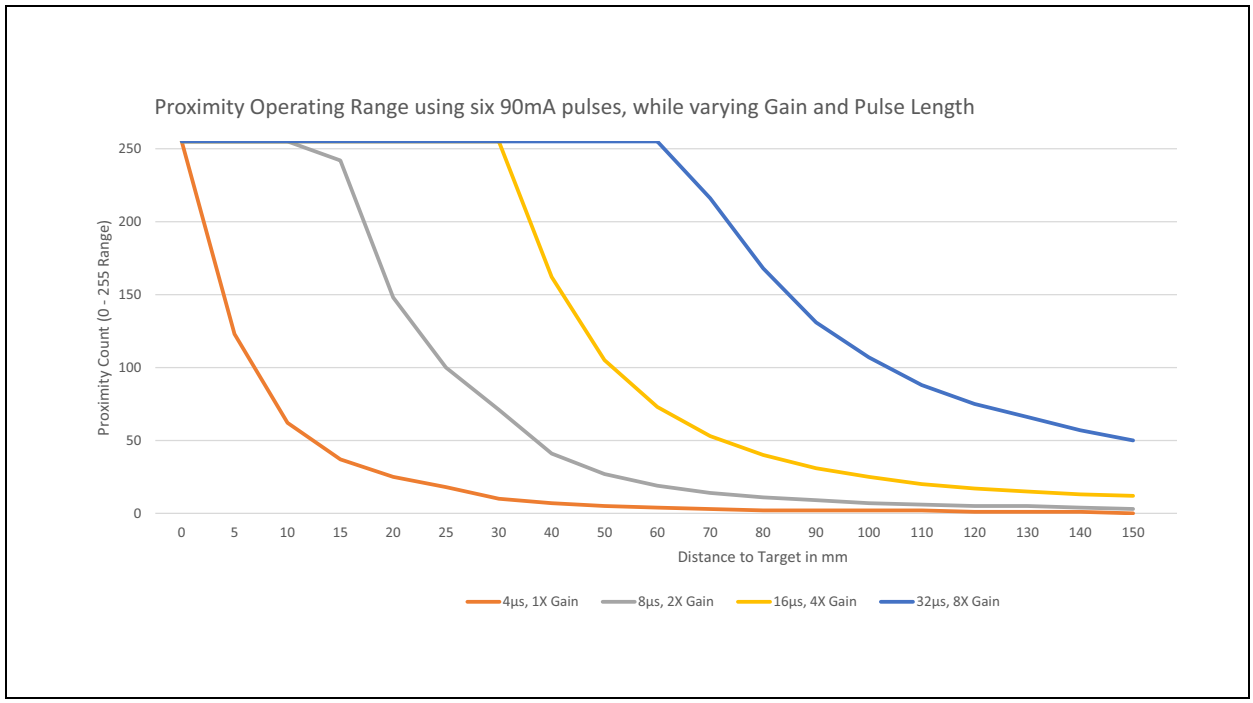
Figure 15:
Typical Proximity Angular Response



Note(s):

1. Pitch = X/Z Plane
2. Yaw = Y/Z Plane

Figure 16:
Proximity Operation of TMD2725



Proximity Operation: By varying Gain, LED drive current, number of LED pulses and LED pulse duration the proximity detection range can be adjusted.

Detailed Description

Proximity

Proximity results are affected by three fundamental factors: the integrated IR LED emission, IR reception, and environmental factors, including target distance and surface reflectivity.

The IR reception signal path begins with IR detection from a photodiode and ends with the 8-bit proximity result in PDATA register. Signal from the photodiode is amplified, and offset adjusted to optimize performance. Offset correction or cross-talk compensation is accomplished by adjustment to the POFFSET register.

The analog circuitry of the device applies the offset value as a subtraction to the signal accumulation; therefore a positive offset value has the effect of decreasing the results.

Ambient Light Sensing, ALS

The ALS reception signal path begins as photodiodes receive filtered light and ends with the 16-bit results in the PHOTOPICL/H and ALS_IRL/H registers. The Photopic photodiode is filtered with a UV and IR filter. The ALS_IR photodiode is filtered to receive only IR. Signal from the photodiodes simultaneously accumulate for a period of time set by the value in ATIME before the results are available. Gain is adjustable from 1x to 64x to facilitate operation over a wide range of lighting conditions. Custom LUX equations are used to calculate the amount of ambient light, as well as, determine the light type (e.g. LED, fluorescent, incandescent, etc.) using the two ALS results.

I^2C Characteristics

The device uses I^2C serial communication protocol for communication. The device supports 7-bit chip addressing and both standard and fast clock frequency modes with a chip address of 0x39. Read and Write transactions comply with the standard set by Philips (now NXP).

Internal to the device, an 8-bit buffer stores the register address location of the desired byte to read or write. This buffer auto-increments upon each byte transfer and is retained between transaction events (I.e. valid even after the master issues a STOP command and the I^2C bus is released). During consecutive Read transactions, the future/repeated I^2C Read transaction may omit the memory address byte normally following the chip address byte; the buffer retains the last register address + 1.

I²C Write Transaction

A Write transaction consists of a START, CHIP-ADDRESS WRITE, REGISTER-ADDRESS, DATA BYTE(S), and STOP. Following each byte (9TH clock pulse) the slave places an ACKNOWLEDGE/ NOT-ACKNOWLEDGE (ACK/NACK) on the bus. If NACK is transmitted by the slave, the master may issue a STOP.

I²C Read Transaction

A Read transaction consists of a START, CHIP-ADDRESS WRITE, REGISTER-ADDRESS, START, CHIP-ADDRESS READ, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9TH clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

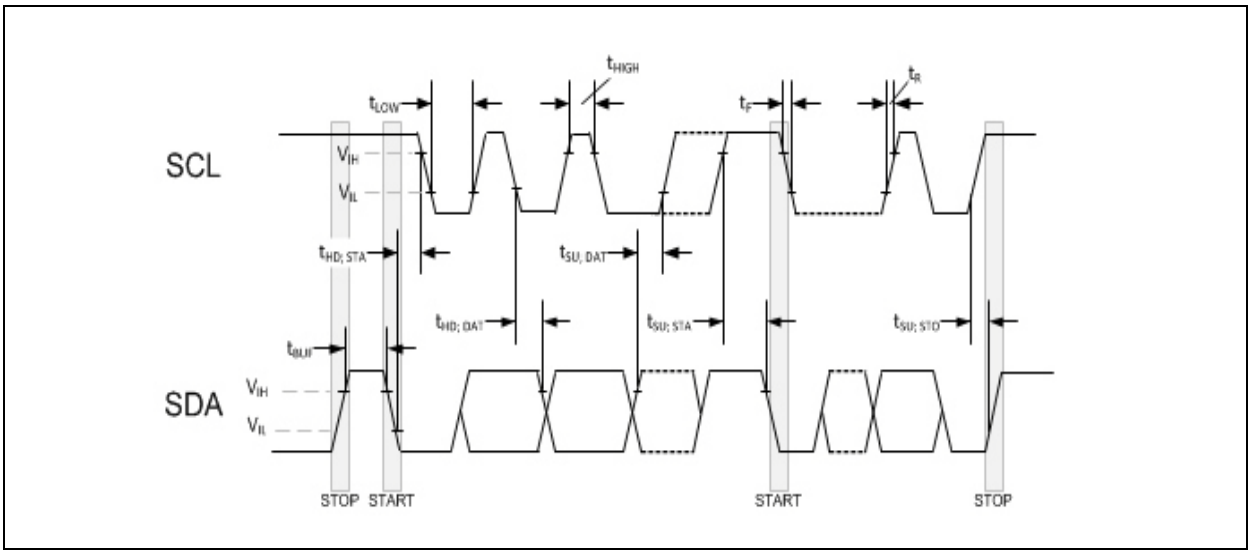
Alternately, if the previous I²C transaction was a Read, the internal register address buffer is still valid, allowing the transaction to proceed without "re"-specifying the register address. In this case the transaction consists of a START, $CHIP\text{-}ADDRESS_{READ}$, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9^{TH} clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

The I²C bus protocol was developed by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification at:

http://www.i2c-bus.org/references/

Timing Diagrams

Figure 17:
I²C Timing



Principles of Operation

System State Machine

An internal state machine provides system control of the ALS, proximity detection, and power management features of the device. At power up, an internal power-on-reset initializes the device and puts it in a lowpower Sleep state. When a write on I^2C bus to the Enable register (0x80) PON bit is set, the device transitions to the Idle state. If PON is disabled, the device will return to the Sleep state to save power. Otherwise, the device will remain in the Idle state until a Proximity or ALS function is enabled. Once enabled, the device will execute the ALS, Proximity and Wait states in sequence as indicated in Figure 18 and Figure 19. Upon completion, the device will automatically begin a new ALS-Prox-Wait cycle as long as PON and either PEN or AEN remain enabled. If the Prox or ALS function generates an interrupt and the Sleep-After-Interrupt (SAI) feature is enabled, the device will transition to the Sleep state and remain in a low-power mode until an I^2C command is received clearing the interrupts in the STATUS register. See Interrupts for additional information.

Figure 18:
Detailed State Diagram

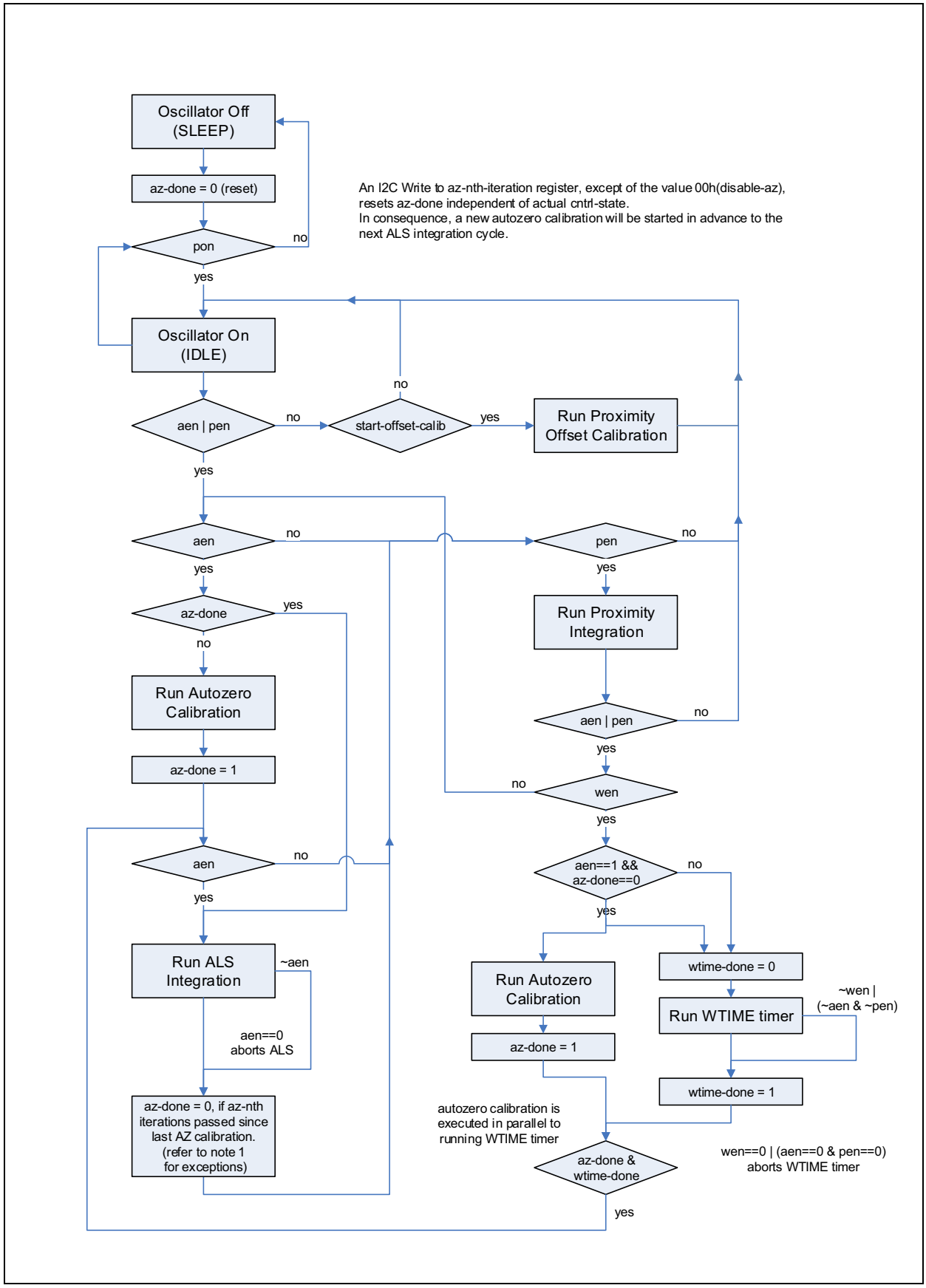
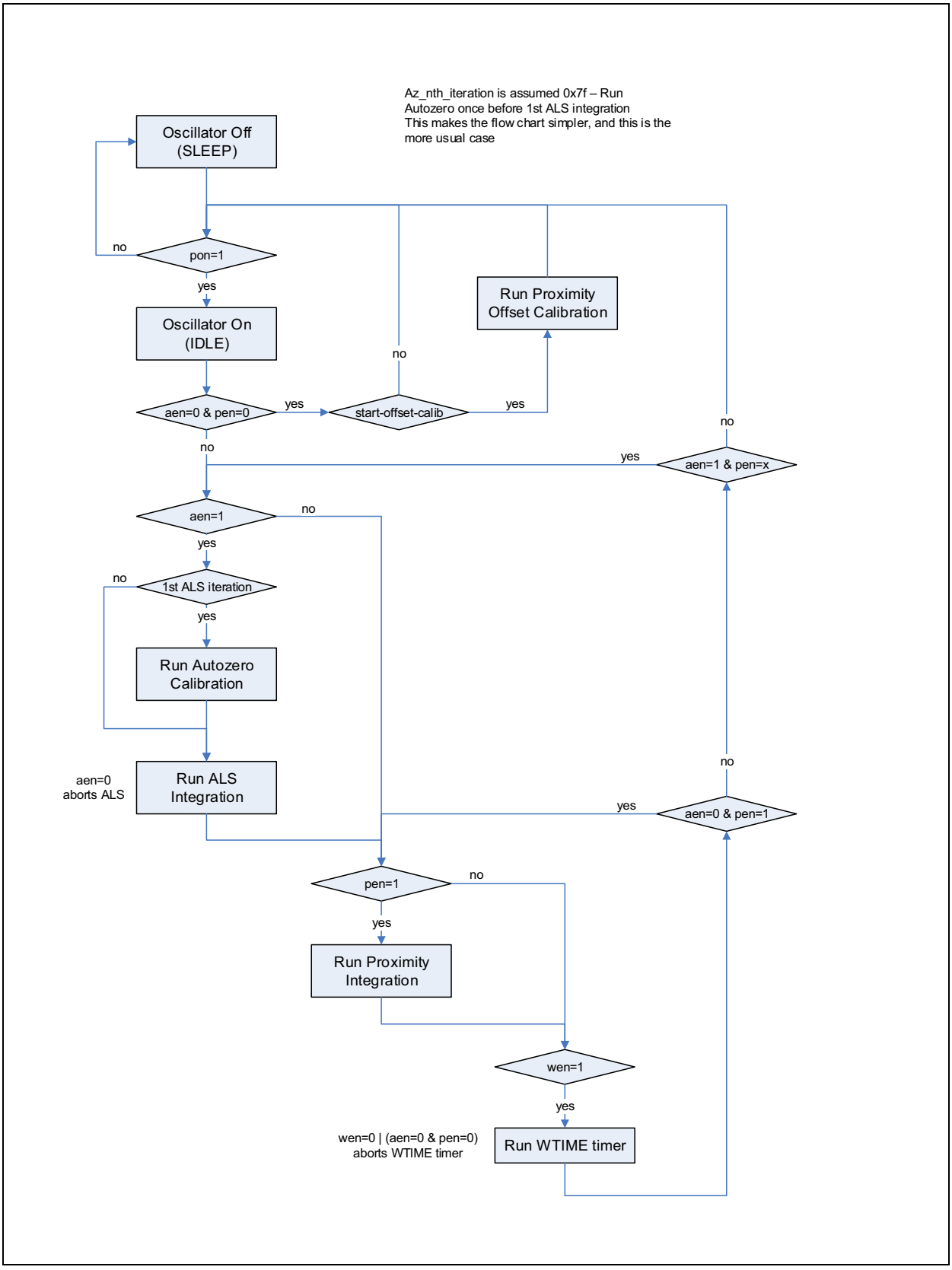


Figure 19:
Simplified State Diagram



Register Description

Register Overview

Figure 20:
Register Overview (the module address is 0x39)

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0x80	ENABLE					WEN	PEN	AEN	PON
0x81	ATIME								
0x82	PTIME								
0x83	WTIME								
0x84	AILTL								
0x85	AILTH								
0x86	AIHTL								
0x87	AIHTH								
0x88	PILT								
0x8A	PIHT								
0x8C	PERS	PPERS				APERS			
0x8D	CFG0						WLONG		
0x8E	PCFG0	PPULSE_LEN		PPULSE					
0x8F	PCFG1	PGAIN			PLDRIVE				
0x90	CFG1							AGAIN	
0x91	REVID						REV_ID		
0x92	ID	ID							
0x93	STATUS	ASAT	PSAT	PINT	AINT	CINT		PSAT_ REFLECTIVE	PSAT_ AMBIENT
0x94	PHOTOPICL								
0x95	PHOTOPICH								
0x96	ALS_IRL								
0x97	ALS_IRH								
0x9C	PDATA								
0x9F	CFG2						AGAINL		

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0xAB	CFG3	INT_ READ_ CLEAR			SAI				
0xC0	POFFSETL								
0xC1	POFFSETH								POFFSET_ SIGN
0xD7	CALIB			ELECTRICAL_ CALIBRATION					START_ OFFSET_ CALIB
0xD9	CALIBCFG	BINSRCH_TARGET				DCAVG_ AUTO_ OFFSET_ ADJUST	PRX_DATA_AVG		
0xDC	CALIBSTAT								CALIB_ FINISHED
0xDD	INTENAB	ASIEN	PSIEN	PIEN	AIEN	CIEN			

Detailed Register Description

Enable Register (Address 0x80)

Figure 21:
Enable Register

Addr: 0x80		Enable		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	RESERVED	0	RW	Reserved.
3	WEN	0	RW	This bit activates the wait feature. Active high.
2	PEN	0	RW	This bit activates the proximity detection. Active high.
1	AEN	0	RW	This bit actives the ALS function. Active high. *Set AEN=1 and PON=1 in the same command to ensure auto-zero function is run prior to the first measurement.
0	PON	0	RW	This field activates the internal oscillator and ADC channels. Active high.

Before activating AEN or PEN, preset each applicable operating mode registers and bits.

ATIME Register (Address 0x81)

Figure 22:
ATIME Register

Addr: 0x81		ATIME					
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**			
7:0	ATIME	0x00	RW	ALS value that specifies the integration time in 2.81ms intervals. 0x00 indicates 2.8ms. The maximum ALS value depends on the integration time. For every 2.81ms, the maximum value increases by 1024. This means that to be able to reach ALS full scale, the integration time has to be at least 64*2.8ms.			
				Value	**Integration Cycles**	**Integration Time**	**Maximum ALS Value**
				0x00	1	2.8ms	1023
				0x01	2	5.6ms	2047
				…	…	…	…
				0x3F	64	180ms	65535
				…	…	…	…
				0xFF	256	719ms	65535

The ATIME register controls the integration time of the ALS ADCs. The timer is implemented with a down counter with 0x00 as the terminal count. The timer is clocked at a 2.8ms nominal rate. Loading 0x00 will generate a 2.8ms integration time, loading 0x01 will generate a 5.6ms integration time, and so forth. The RC oscillator runs at 8MHz nominal rate. This gets divided by 11 to generate the integration clock of 727kHz. One count in ATIME (nominal 2.8ms) are 2.81ms. This is 2048 integration clock cycles: 125ns*11*8*256=2.81ms.

PTIME Register (Address 0x82)

Figure 23:
PTIME Register

Addr: 0x82		PTIME		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PTIME	0x1F	RW	This register defines the duration of 1 Prox Sample, which is (PTIME + 1)*88µs.

WTIME Register (Address 0x83)

Figure 24:
WTIME Register

<table>
<tr><th colspan="2">Addr: 0x83</th><th colspan="3">WTIME</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th>Bit Description</th></tr>
<tr><td rowspan="8">7:0</td><td rowspan="8">WTIME</td><td rowspan="8">0x00</td><td rowspan="8">RW</td><td>Value that specifies the wait time between ALS cycles in 2.81ms increments.</td></tr>
<tr><td>
<table>
<tr><th>Value</th><th>Increments</th><th>Wait Time</th></tr>
<tr><td>0x00</td><td>1</td><td>2.8ms (33.8ms)</td></tr>
<tr><td>0x01</td><td>2</td><td>5.6ms (67.6ms)</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>0x3F</td><td>64</td><td>180ms (2.16s)</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>0xFF</td><td>256</td><td>719ms (8.65s)</td></tr>
</table>
</td></tr>
</table>

The wait timer is implemented using a down counter. Wait time = (value +1) x 2.8ms. If WLONG is enabled then Wait time = (value +1) x 2.8ms. x 12.

AILTL Register (Address 0x84)

Figure 25:
AILTL Register

Addr: 0x84		AILTL		
Bit	Bit Name	Default	Access	Bit Description
7:0	AILTL	0x00	RW	This register sets the low byte of the LOW ALS threshold.

The photopic channel is compared against low-going 16-bit threshold value set by AILTL and AILTH.

AILTH Register (Address 0x85)

Figure 26:
AILTH Register

Addr: 0x85		AILTH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	AILTH	0x00	RW	This register sets the high byte of the LOW ALS threshold.

The photopic channel is compared against low-going 16-bit threshold value set by AILTL and AILTH.
The contents of the AILTH and AILTL registers are combined and treated as a sixteen bit threshold value. If the value generated by the photopic channel is below the AILTL/H threshold and the APERS value is reached, the AINT bit is asserted. If AIEN is set, then the INT pin will also assert.
When setting the 16-bit ALS threshold AILTL must be written first, immediately follow by AILTH. Internally, the lower 8-bits are buffered until the upper 8-bits are written. As the upper 8-bits are written both the high and low bytes are simultaneously latched as a 16-bit value.

AIHTL Register (Address 0x86)

Figure 27:
AIHTL Register

Addr: 0x86		AIHTL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	AIHTL	0x00	RW	This register sets the low byte of the HIGH ALS threshold.

The photopic channel is compared against high-going 16-bit threshold value set by AIHTL and AIHTH.
The contents of the AIHTH and AIHTL registers are combined and treated as a sixteen bit threshold value. If the value generated by the photopic channel is above the AIHTL/H threshold and the APERS value is reached, the AINT bit is asserted. If AIEN is set, then the INT pin will also assert. When setting the 16-bit ALS threshold AIHTL must be written first, immediately follow by AIHTH. Internally, the lower 8-bits are buffered until the upper 8-bits are written. As the upper 8-bits are written both the high and low bytes are simultaneously latched as a 16-bit value.

AIHTH Register (Address 0x87)

Figure 28:
AIHTH Register

Addr: 0x87		AIHTH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	AIHTH	0x00	RW	This register sets the high byte of the HIGH ALS threshold.

The photopic channel is compared against high-going 16-bit threshold value set by AIHTL and AIHTH.
The contents of the AIHTH and AIHTL registers are combined and treated as a sixteen bit threshold value. If the value generated by the photopic channel is above the AIHTL/H threshold and the APERS value is reached, the AINT bit is asserted. If AIEN is set, then the INT pin will also assert.
When setting the 16-bit ALS threshold AIHTL must be written first, immediately follow by AIHTH. Internally, the lower 8-bits are buffered until the upper 8-bits are written. As the upper 8-bits are written both the high and low bytes are simultaneously latched as a 16-bit value.

PILT Register (Address 0x88)

Figure 29:
PILT Register

Addr: 0x88		PILT		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PILT	0x00	RW	This register sets the Proximity ADC channel low threshold.

The proximity channel is compared against low-going 8-bit threshold value set by PILT.
If the value generated by the Proximity channel is below the PILT threshold and the PPERS value is reached, the PINT bit is asserted. If PIEN is set, then the INT pin will also assert.

PIHT Register (Address 0x8A)

Figure 30:
PIHT Register

Addr: 0x8A		PIHT		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PIHT	0x00	RW	This register sets the Proximity ADC channel high threshold.

The proximity channel is compared against high-going 8-bit threshold value set by PIHT.
If the value generated by the Proximity channel is above the PIHT threshold and the PPERS value is reached, the PINT bit is asserted. If PIEN is set, then the INT pin will also assert.

PERS Register (Address 0x8C)

Figure 31:
PERS Register

Addr: 0x8C		PERS			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:4	PPERS	0x00	RW	This register sets the Proximity persistence filter.	
				Value	**Interrupt**
				0	Every Proximity Cycle
				1	Any value outside PILT/PIHT thresholds
				2	2 consecutive proximity values out of range
				3	3 consecutive proximity values out of range
				…	….
				15	15 consecutive proximity values out of range

Addr: 0x8C		PERS			
Bit	Bit Name	Default	Access	Bit Description	
3:0	APERS	0x0	RW	This register sets the ALS persistence filter.	
				0	Every ALS Cycle
				1	Any value outside ALS thresholds
				2	2 consecutive ALS values out of range
				3	3 consecutive ALS values out of range
				4	5 consecutive ALS values out of range
				5	10 consecutive ALS values out of range
				6	15 consecutive ALS values out of range
				7	20 consecutive ALS values out of range
				…	…
				13	50 consecutive ALS values out of range
				14	55 consecutive ALS values out of range
				15	60 consecutive ALS values out of range

The frequency of consecutive proximity channel results outside of threshold limits are counted; this count value is compared against the PPERS value. If the counter is equal to the PPERS value an interrupt is asserted. Any time a proximity channel result is inside the threshold values the counter is cleared.
The frequency of consecutive photopic channel results outside of threshold limits are counted; this count value is compared against the APERS value. If the counter is equal to the APERS setting an interrupt is asserted. Any time a photopic channel result is inside the threshold values the counter is cleared.

CFG0 Register (Address 0x8D)

Figure 32:
CFG0 Register

Addr: 0x8D		CFG0		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	Reserved	10000	RW	This field must be set to the default value.
2	WLONG	0	RW	When Wait Long is asserted the wait period as set by WTIME is increased by a factor of 12.
1:0	Reserved	0	RW	This field must be set to the default value.

The wait timer is implemented using a down counter.
Wait time = (value +1) x 2.8ms. If WLONG is enabled then
Wait time = (value +1) x 2.8ms x 12.

PCFG0 Register (Address 0x8E)

Figure 33:
PCFG0 Register

Addr: 0x8E		PCFG0			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:6	PPULSE_LEN	01	RW	Proximity Pulse Length	
				Value	**Pulse Length**
				0	4µs
				1	8µs
				2	16µs
				3	32µs
5:0	PPULSE	001111	RW	Maximum Number of Pulses in a single proximity cycle.	
				Value	**Maximum Number of Pulses**
				0	1
				1	2
				2	3
				…	…
				63	64

The PPULSE_LEN field sets the width of all IR LED pulses within the proximity cycle. Longer pulses result in increased proximity range and typically result in less electrical noise generated in the analog front end. However, a setting of 8µs is recommended because less cumulative noise is generated during a proximity cycle.

The PPULSE field sets the maximum number of IR LED pulses that may occur in a proximity cycle. The proximity engine will automatically continue to add IR LED pulses, up to the value set in PPULSE or if a near-saturation condition occurs.

The dynamic range of the sensor is automatically adjusted to detect distant targets as well as prevent saturation from close targets.

This operation also reduces power consumption because proximity integration period is automatically shortened when a target is either to close or far from the sensor.

PCFG1 Register (Address 0x8F)

Figure 34:
PCFG1 Register

<table>
<tr><th colspan="2">Addr: 0x8F</th><th colspan="4">PCFG1</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="3">Bit Description</th></tr>
<tr><td rowspan="5">7:6</td><td rowspan="5">PGAIN</td><td rowspan="5">10</td><td rowspan="5">RW</td><td colspan="3">This field sets the gain of the proximity IR sensor.</td></tr>
<tr><td>Gain</td><td>Value</td><td>Bit Field</td></tr>
<tr><td>1x</td><td>0</td><td>00b</td></tr>
<tr><td>2x</td><td>1</td><td>01b</td></tr>
<tr><td>4x</td><td>2</td><td>10b</td></tr>
<tr><td>8x</td><td>3</td><td>11b</td></tr>
<tr><td>5</td><td>Reserved</td><td>0</td><td>RW</td><td colspan="3">Reserved</td></tr>
<tr><td rowspan="8">4:0</td><td rowspan="8">PLDRIVE</td><td rowspan="8">0</td><td rowspan="8">RW</td><td colspan="3">This field sets the drive strength of the IR LED current. Values are approximate; actual current through LED is factory trimmed to normalize IR intensity.</td></tr>
<tr><td colspan="2">Value</td><td>LED Current</td></tr>
<tr><td colspan="2">0</td><td>6mA</td></tr>
<tr><td colspan="2">1</td><td>12mA</td></tr>
<tr><td colspan="3">i_{LED} = 6(PLDRIVE +1) mA</td></tr>
<tr><td colspan="2">30</td><td>186mA</td></tr>
<tr><td colspan="2">31</td><td>192mA</td></tr>
</table>

CFG1 Register (Address 0x90)

Figure 35:
CFG1 Register

Addr: 0x90		CFG1			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:2	Reserved	000000	RW	Reserved	
1:0	AGAIN	00	RW	This field sets the gain of the ALS sensor.	
				Value	**Gain**
				0	1x
				1	4x
				2	16x
				3	64x

REVID Register (Address 0x91)

Figure 36:
REVID Register

Addr: 0x91		REVID		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	Reserved	...	RO	Reserved
2:0	REV_ID	Rev	RO	Device revision number

ID Register (Address 0x92)

Figure 37:
ID Register

Addr: 0x92		ID		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:2	ID	111001	RO	Device type identification.
1:0	Reserved	...	RO	Reserved

Status Register (Address 0x93)

Figure 38:
Status Register

Addr: 0x93		Status Register		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ASAT	0	R, SC	The Analog Saturation flag signals that the ALS results may be unreliable due to saturation of the AFE.
6	PSAT	0	R, SC	The Proximity Saturation flag indicates that an ambient- or reflective-saturation event occurred during a previous proximity cycle.
5	PINT	0	R, SC	The Proximity Interrupt flag indicates that proximity results have exceeded thresholds and persistence settings.
4	AINT	0	R, SC	The ALS Interrupt flag indicates that ALS results (photopic channel) have exceeded thresholds and persistence settings.
3	CINT	0	R, SC	The Calibration Interrupt flag indicates that calibration has completed.
2	Reserved	0	R, SC	Reserved
1	PSAT_REFLECTIVE	0	R, SC	The Reflective Proximity Saturation Interrupt flag signals that the AFE has saturated during the IR LED active portion of proximity integration.
0	PSAT_AMBIENT	0	R, SC	The Ambient Proximity Saturation Interrupt flag signals that the AFE has saturated during the IR LED inactive portion of proximity integration.

All flags in this register can be cleared by setting the bit high. Alternatively, if the CFG3.int_read_clear bit is set, then simply reading this register automatically clears all eight flags.

PHOTOPICL Register (Address 0x94)

Figure 39:
PHOTOPICL Register

Addr: 0x94		PHOTOPICL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PHOTOPICL	0x00	RO	This register contains the low byte of the 16-bit photopic channel data.

PHOTOPICH Register (Address 0x95)

Figure 40:
PHOTOPICH Register

Addr: 0x95		PHOTOPICH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PHOTOPICH	0x00	RO	This register contains the high byte of the 16-bit photopic channel data.

ALS_IRL Register (Address 0x96)

Figure 41:
ALS_IRL Register

Addr: 0x96		ALS_IRL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ALS_IRL	0x00	RO	This register contains the low byte of the 16-bit IR channel data.

ALS_IRH Register (Address 0x97)

Figure 42:
ALS_IRH Register

Addr: 0x97		ALS_IRH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ALS_IRH	0x00	RO	This register contains the high byte of the 16-bit IR channel data.

PDATA Register (Address 0x9C)

Figure 43:
PDATA Register

Addr: 0x9C		PDATA		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PDATA	0x00	RO	This register contains the 8-bit proximity channel data.

CFG2 Register (Address 0x9F)

Figure 44:
CFG2 Register

Addr: 0x9F		CFG2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	Reserved	0	RW	Reserved
2	AGAINL	1	RW	This bit adjusts the overall ALS gain factor. Reset to 0 causes the overall gain to be divided by 2. ALS gain will be unaffected when set to 1.
1:0	Reserved	0	RW	Reserved

The ALS gain can be adjusted using by setting the two AGAIN bits as well as the AGAINL bit which yields an overall range from ½ x to 64x.

Figure 45:
AGAIN Range

AGAIN[1]	AGAIN[0]	AGAINL	Overall ALS Gain
0	0	0	½
0	0	1	1
0	1	0	2
0	1	1	4
1	0	0	8
1	0	1	16
1	1	0	32
1	1	1	64

CFG3 Register (Address 0xAB)

Figure 46:
CFG3 Register

<table>
<tr><th colspan="2">Addr: 0xAB</th><th colspan="4">CFG3</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="4">Bit Description</th></tr>
<tr><td>7</td><td>INT_READ_CLEAR</td><td>0</td><td>RW</td><td colspan="4">If the Interrupt-Clear-by-Read bit is set, then all flag bits in the STATUS register will be reset whenever the STATUS register is read over I²C.</td></tr>
<tr><td>6:5</td><td>Reserved</td><td>0x2</td><td>RW</td><td colspan="4">Reserved</td></tr>
<tr><td rowspan="6">4</td><td rowspan="6">SAI</td><td rowspan="6">0</td><td rowspan="6">RW</td><td colspan="4">The Sleep After Interrupt bit is used to place the device into a low power mode upon an interrupt pin assertion.</td></tr>
<tr><td>PON</td><td>SAI</td><td>INT</td><td>Oscillator</td></tr>
<tr><td>0</td><td>X</td><td>X</td><td>OFF</td></tr>
<tr><td>1</td><td>0</td><td>X</td><td>ON</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>ON</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>OFF</td></tr>
<tr><td>3:0</td><td>Reserved</td><td>0xC</td><td>RW</td><td colspan="4">Reserved</td></tr>
</table>

The SAI bit sets the device operational mode following the completion of an ALS or proximity cycle. If AINT and AIEN are both set or if PINT and PIEN are both set, causing an interrupt on the INT pin, and the SAI bit is set, then the oscillator will deactivate. The Device will appear as if PON = 0, however, PON will read as 1. The device can only be reactivated (oscillator enabled) by clearing the interrupts in the STATUS register.

POFFSETL Register (Address 0xC0)

Figure 47:
POFFSETL Register

Addr: 0xC0		POFFSETL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	POFFSETL	0x00	RW	This register contains the magnitude portion of proximity offset adjust value.

Typically, optical and/or electrical crosstalk negatively influence proximity operation and results. The POFFSETL/POFFSETH registers provide a mechanism to remove system crosstalk from the proximity data. POFFSETL and POFFSETH contains the magnitude and sign of a value which adjusts PDATA generated in the AFE. An offset value in the range of ± 255 is possible.

POFFSETH Register (Address 0xC1)

Figure 48:
POFFSETH Register

Addr: 0xC1		POFFSETH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:1	Reserved	0	RW	Reserved
0	POFFSET_SIGN	0	RW	This register contains the sign portion of proximity offset adjust value.

CALIB Register (Address 0xD7)

Figure 49:
CALIB Register

Addr: 0xD7		CALIB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	Reserved	0	RO	Reserved
5	ELECTRICAL_ CALIBRATION	0	RW	Selects proximity calibration type. 1 = electrical offset only. 0 = calibration compensates for electrical and optical crosstalk.
4:1	Reserved	0	RW	Reserved
0	START_OFFSET_ CALIB	0	RW	Set to 1 to start a calibration sequence.

Proximity response in systems with electrical and optical crosstalk may be improved by using the calibration feature. Optical crosstalk is caused when the photodiode receives a small portion of the LED IR which was unintentionally reflected by a surface other than the target. Electrical offset is caused by electrical disturbance in the sensor AFE, and also influences the proximity result. The calibration routine adjusts the value in registers C0 and C1 until the proximity result is as close to BINSRCH_TARGET as possible without becoming zero.

Optical and electrical calibration function identically, except that during an electrical calibration the proximity photodiode is disconnected from the AFE.

Upon power-up, the device always automatically performs an electrical calibration. However, an electrical calibration can be initiated anytime by setting the ELECTRICAL_CALIBRATION and START_OFFSET_CALB bits.

To perform an optical (and electrical) calibration do not set the ELECTRICAL_CALIBRATION bit when setting the START_ OFFSET_CALIB. The CINT flag will assert after calibration has finished.

Upon completion Proximity offset registers are automatically loaded with calibration result.

CALIBCFG Register (Address 0xD9)

Figure 50:
CALIBCFG Register

Addr: 0xD9		CALIBCFG			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:5	BINSRCH_ TARGET	010	RW	Proximity Result Target	
				Value	**PDATA Target**
				0	0
				1	1
				2	3
				3	7
				4	15
				5	31
				6	63
				7	127
4	Reserved	0	RW	Reserved	
3	AUTO_ OFFSET_ADJ	0	RW	The Proximity Auto Offset Adjust bit causes the value in POFFSETL register to decrement when PDATA equals zero at the completion of the proximity cycle.	
2:0	PROX_AVG	0	RW	The Proximity Averaging field defines the number of ADC samples collected and averaged during a cycle which become the proximity result.	
				Value	**Sample Size**
				0	Disable
				1	2
				2	4
				3	8
				4	16
				5	32
				6	64
				7	128

The binary search target field is used by the calibration feature to set the baseline value for PDATA when no target is present. For example, calibration of a device in open air, with no target,

and BINSEARCH_TARGET setting of 4 causes the PDATA value will be approximately 15 counts. This feature is useful because it forces PDATA result to always be above zero.
The PROX_AVG field sets the number of ADC samples that are averaged to calculate the PDATA result.

CALIBSTAT Register (Address 0xDC)

Figure 51:
CALIBSTAT Register

Addr: 0xDC		CALIBSTAT		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:1	Reserved	0	RW	Reserved
0	CALIB_FINISHED	0	RW	This flag indicates that calibration has finished. It can only be cleared by setting this bit high.

INTENAB Register (Address 0xDD)

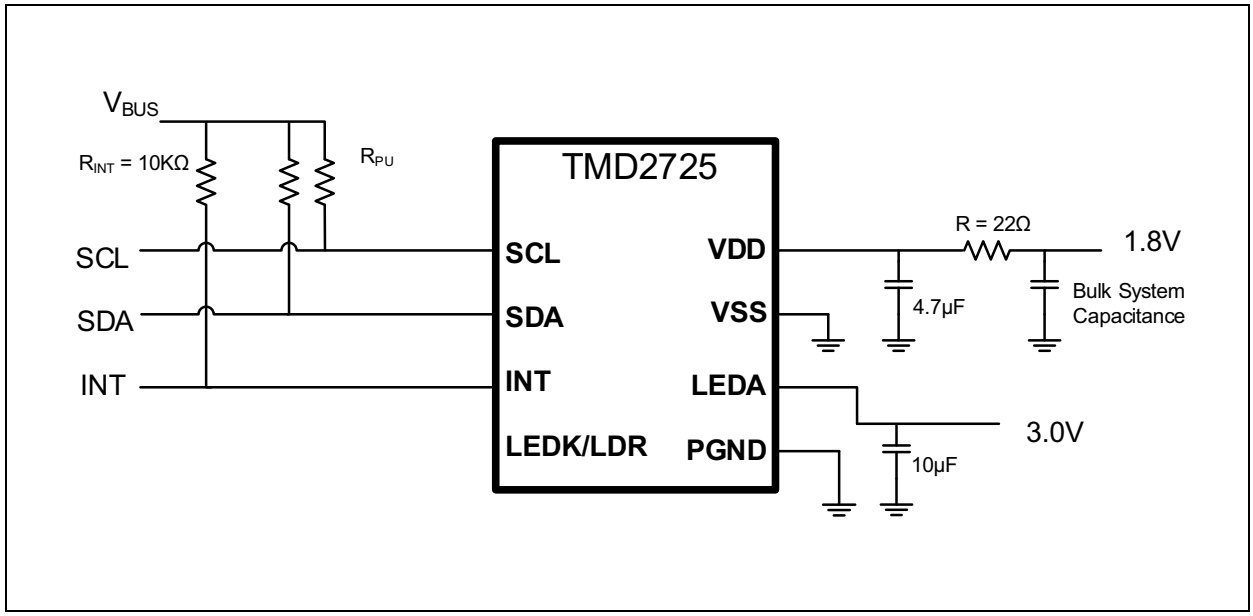
Figure 52:
INTENAB Register

Addr: 0xDD		INTENAB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ASIEN	0	RW	ALS Saturation Interrupt Enable
6	PSIEN	0	RW	Proximity Saturation Interrupt Enable
5	PIEN	0	RW	Proximity Interrupt Enable
4	AIEN	0	RW	ALS Interrupt Enable
3	CIEN	0	RW	Calibration Interrupt Enable
2:0	Reserved	0	RW	Reserved

Application Information

Schematic

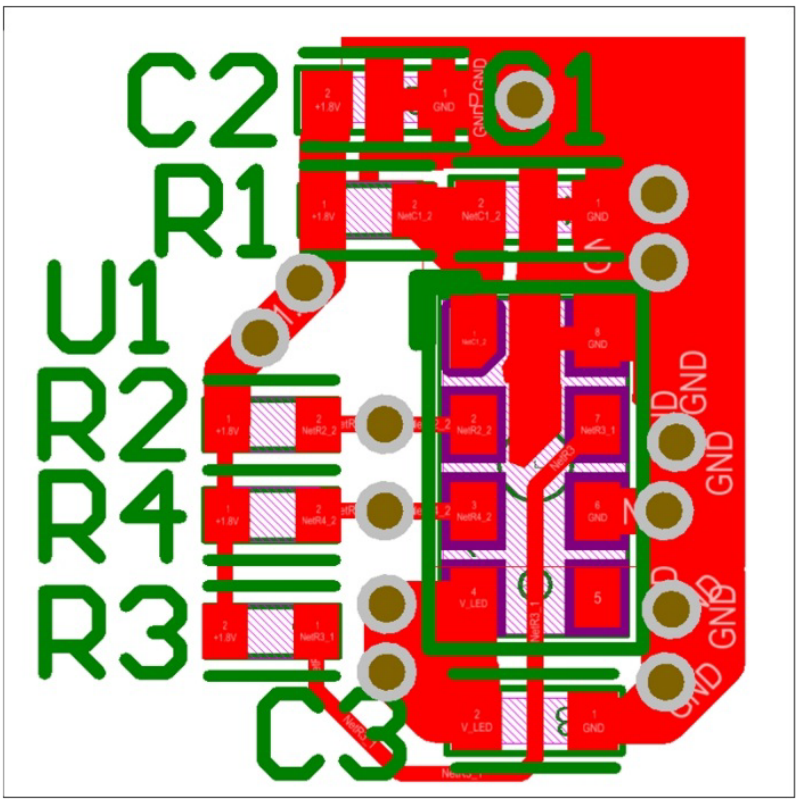
Figure 53:
Typical Applications Circuit



Typical Applications Circuit: It is important to place the 4.7µF (VDD) and 10µF (LEDA) capacitors at the package pins.

PCB Layout

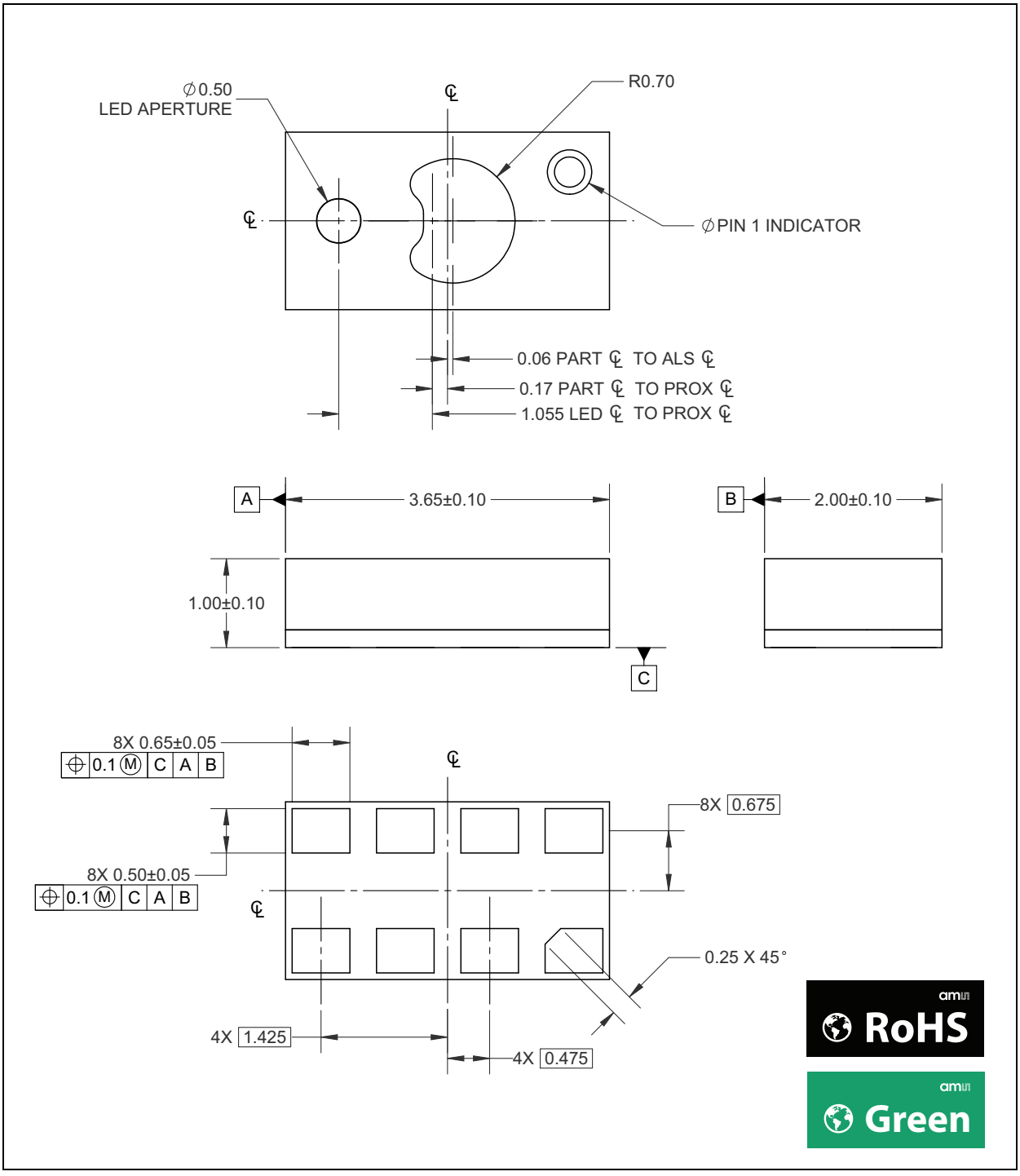
Figure 54:
Typical Applications Circuit



The dominant factor governing device performance is the component placement, not necessarily component value. The placement of the decoupling capacitor, C1, is the most critical. Place the component on the same side of PCB as device as shown in the figure above. Make connection as close as possible to minimize series inductance and resistance. This is critical.

Package Drawings & Markings

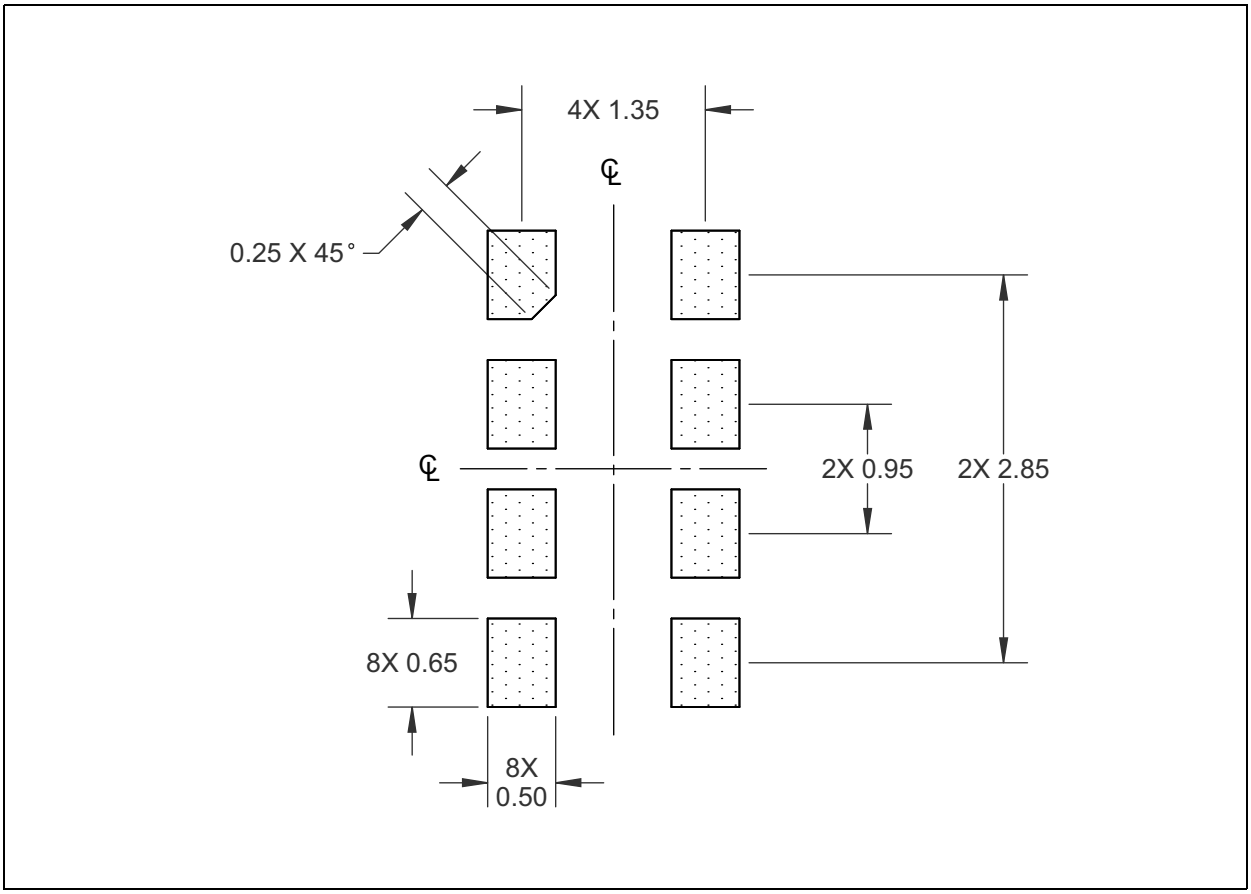
Figure 55:
Package Drawings



Note(s):

1. All linear dimensions are in millimeters.
2. Contact finish is Au.
3. This package contains no lead (Pb).
4. This drawing is subject to change without notice.

Figure 56:
Recommended PCB Layout

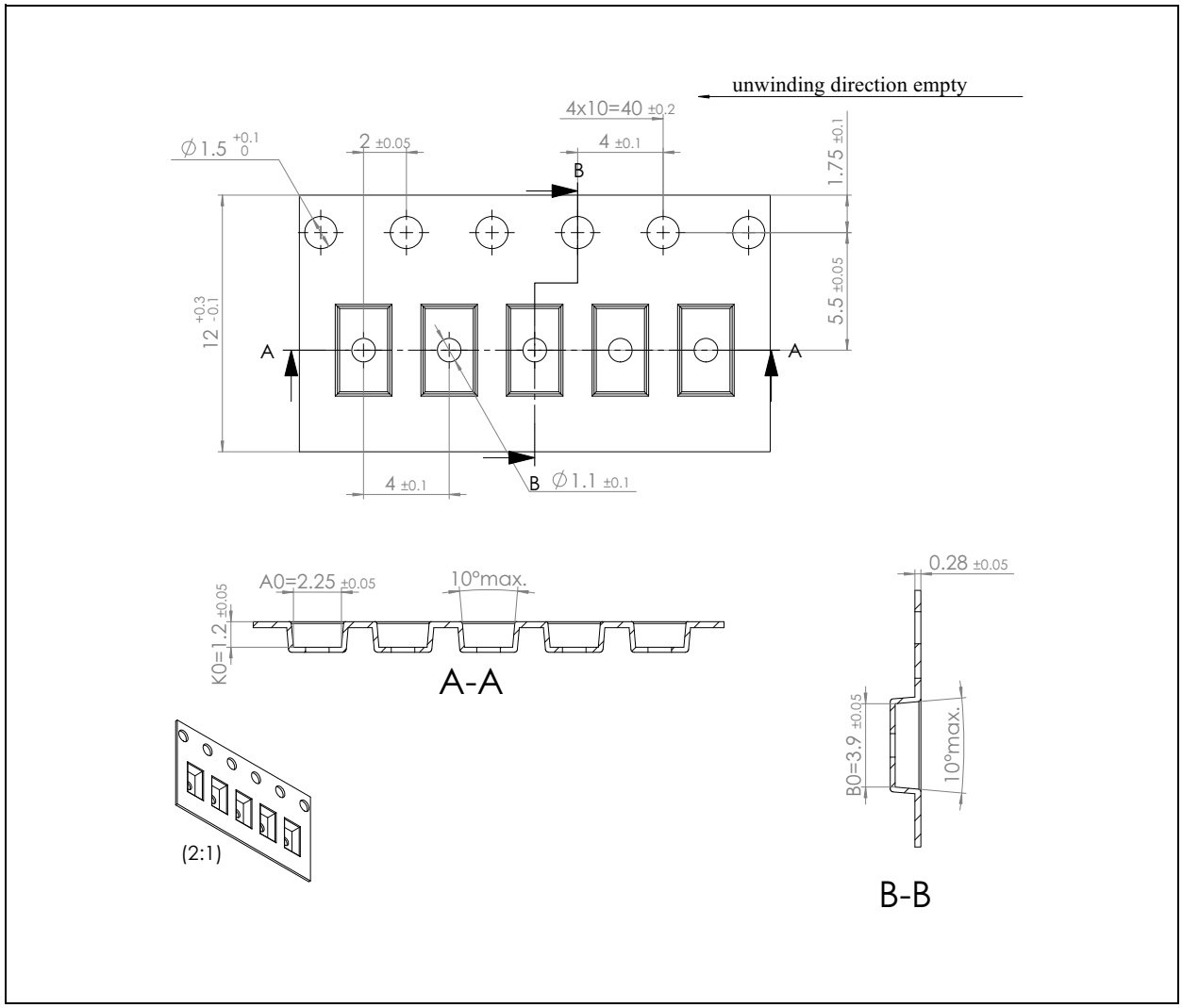


Note(s):

1. All dimensions are in millimeters.
2. Dimension tolerances are 0.05mm unless otherwise noted.
3. This drawing is subject to change without notice.

Tape & Reel Information

Figure 57:
Tape and Reel Information



Note(s):

1. All linear dimensions are in millimeters.
2. For missing tolerances and dimensions, refer to EIA-481.

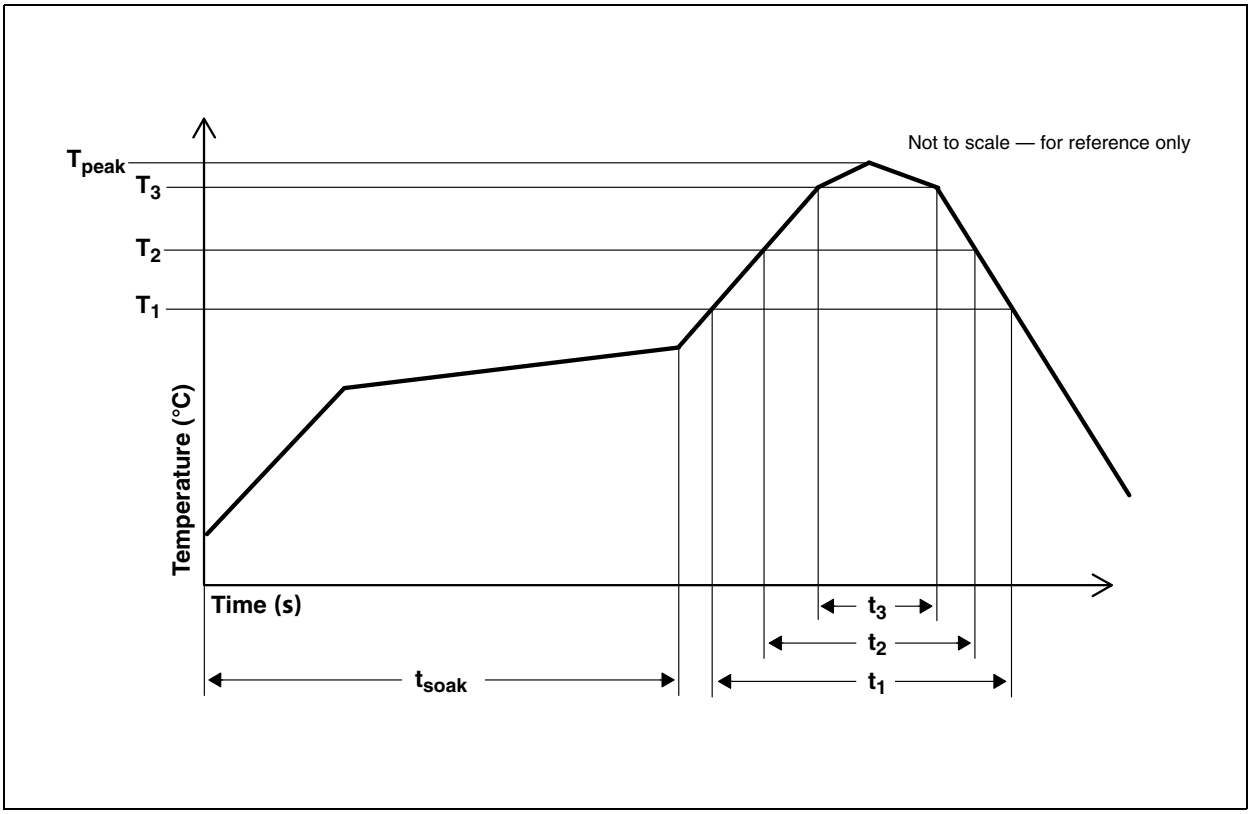
Soldering & Storage Information

The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate. The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Figure 58:
Solder Reflow Profile

Parameter	Reference	Device
Average temperature gradient in preheating		2.5°C/s
Soak time	t_{SOAK}	2 to 3 minutes
Time above 217°C (T_1)	t_1	Max 60s
Time above 230°C (T_2)	t_2	Max 50s
Time above T_{peak} - 10°C (T_3)	t_3	Max 10s
Peak temperature in reflow	T_{peak}	260°C
Temperature gradient in cooling		Max - 5°C/s

Figure 59:
Solder Reflow Profile Graph



Storage Information

Moisture Sensitivity Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping. Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 12 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 12 months
- Ambient Temperature: <40°C
- Relative Humidity: <90%

Rebaking of the devices will be required if the devices exceed the 12 month shelf life and the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

Floor Life

The module has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor Life: 168 hours
- Ambient Temperature: <30°C
- Relative Humidity: <60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

Ordering & Contact Information

Figure 60:
Ordering Information

Ordering Code	I²C Bus	I²C Address	Delivery Form	Delivery Quantity
TMD27253M	1.8V	39h	Tape & Reel (7")	1000 pcs/reel
TMD27253			Tape & Reel (13")	10000 pcs/reel

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Document Status	Product Status	Definition
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Revision Information

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Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

Content Guide