500 kSPS, 8-Channel, Software-Selectable, True Bipolar Input, 12-Bit Plus Sign ADC

Enhanced Product

AD7327-EP

FEATURES

- 12-bit plus sign SAR ADC
- True bipolar input ranges
- Software-selectable input ranges
  - ±10 V, ±5 V, ±2.5 V, 0 V to +10 V
- Military temperature range: −55°C to +125°C
- 500 kSPS throughput rate
- 8 analog input channels with channel sequencer
- Single-ended, true differential, and pseudo differential analog input capability
- High analog input impedance
- Low power: 18 mW
- Temperature indicator
- Full power signal bandwidth: 22 MHz
- Internal 2.5 V reference
- High speed serial interface
- Power-down modes
- Controlled manufacturing baseline
- Single assembly/test site
- 20-lead TSSOP package
- *i*CMOS process technology
- Qualification data available on request

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range: −55°C to +105°C
- Controlled manufacturing baseline
- One assembly/test site
- One fabrication site
- Enhanced product change notification
- Qualification data available on request

GENERAL DESCRIPTION

The AD7327-EP[1] is an 8-channel, 12-bit plus sign successive approximation ADC designed on the *i*CMOS™ (industrial CMOS) process. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no previous generation of high voltage devices achieved. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can accept bipolar input signals while providing increased performance, dramatically reduced power consumption, and reduced package size.

The AD7327-EP can accept true bipolar analog input signals, software-selectable from ±10 V, ±5 V, ±2.5 V, and 0 V to +10 V. Each analog input channel can be independently programmed to one of the four input ranges. The analog input channels on the AD7327-EP can be programmed to be single-ended, true differential, or pseudo differential.

The ADC contains a 2.5 V internal reference. The AD7327-EP also allows external reference operation. If a 3 V reference is applied to the REFIN/OUT pin, the AD7327-EP can accept a true bipolar ±12 V analog input. Minimum ±12 V V_{DD} and V_{SS} supplies are required for the ±12 V input range. The ADC has a high speed serial interface that can operate at throughput rates up to 500 kSPS.

The AD7327-EP is housed in a 20-lead TSSOP with operation specified from −55°C to +125°C. Additional application and technical information can be found in the AD7327 data sheet.

FUNCTIONAL BLOCK DIAGRAM

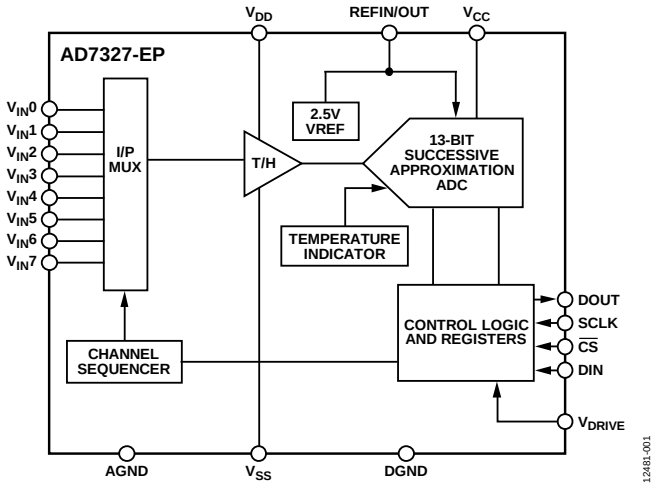

Figure 1.

PRODUCT HIGHLIGHTS

1. The AD7327-EP can accept true bipolar analog input signals, ±10 V, ±5 V, ±2.5 V, and 0 V to +10 V (unipolar).
2. The eight analog inputs can be configured as eight single-ended inputs, four true differential inputs, four pseudo differential inputs, or seven pseudo differential inputs.
3. 500 kSPS serial interface. SPI®-/QSPI™-/DSP-/MICROWIRE™-compatible interface.
4. Low power, 18 mW, at a maximum throughput rate of 500 kSPS.
5. Channel sequencer.

[1] Protected by U.S. Patent No. 6,731,232.

Rev. B
Document Feedback

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9/14—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 12 V to 16.5 V, V_{SS} = −12 V to −16.5 V, V_{CC} = 2.7 V to 5.25 V, V_{DRIVE} = 2.7 V to 5.25 V, V_{REF} = 2.5 V to 3.0 V internal/external, f_{SCLK} = 10 MHz, f_S = 500 kSPS, T_A = T_{MAX} to T_{MIN}, unless otherwise noted.

Table 1.

	B Version				
Parameter[1]	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
DYNAMIC PERFORMANCE					f_{IN} = 50 kHz sine wave
Signal-to-Noise Ratio (SNR)[2]	76			dB	Differential mode, V_{CC} = 4.75 V to 5.25 V
	75.5			dB	Differential mode, V_{CC} < 4.75 V
	72			dB	Single-ended/pseudo differential mode; ±10 V, ±2.5 V and ±5 V ranges, V_{CC} = 4.75 V to 5.25 V
	71.7			dB	Single-ended/pseudo differential mode; 0 V to 10 V V_{CC} = 4.75 V to 5.25 V and all ranges at V_{CC} < 4.75 V
Signal-to-Noise + Distortion (SINAD)[2]	75			dB	Differential mode; ±2.5 V and ±5 V ranges
	74				Differential mode; 0 V to 10 V
		76		dB	Differential mode; ±10 V range
	70.7			dB	Single-ended/pseudo differential mode; ±2.5 V and ±5 V ranges
		72.5		dB	Single-ended/pseudo differential mode; 0 V to +10 V and ±10 V ranges
Total Harmonic Distortion (THD)[2]			−79.3	dB	Differential mode; ±2.5 V and ±5 V ranges
			−78.8	dB	Differential mode; 0 V to 10 V ranges
		−82		dB	Differential mode; ±10 V range
			−76	dB	Single-ended/pseudo differential mode; ±5 V range
			−77.3	dB	Single-ended/pseudo differential mode; ±2.5 V range
		−80		dB	Single-ended/pseudo differential mode; 0 V to +10 V and ±10 V ranges
Peak Harmonic or Spurious Noise (SFDR)[2]			−80	dB	Differential mode; ±2.5 V and ±5 V ranges
			−80	dB	Differential mode; 0 V to 10 V ranges
		−82		dB	Differential mode; ±10 V ranges
			−77.2	dB	Single-ended/pseudo differential mode; ±5 V range
			−78.9		Single-ended/pseudo differential mode; ±2.5 V range
		−79		dB	Single-ended/pseudo differential mode; 0 V to +10 V and ±10 V ranges
Intermodulation Distortion (IMD)[2]					f_A = 50 kHz, f_B = 30 kHz
Second-Order Terms		−88		dB	
Third-Order Terms		−90		dB	
Aperture Delay[3]		7		ns	
Aperture Jitter[3]		50		ps	
Common-Mode Rejection (CMRR)[2]		−79		dB	Up to 100 kHz ripple frequency; see Figure 17
Channel-to-Channel Isolation[2]		−72		dB	f_{IN} on unselected channels up to 100 kHz; see Figure 14
Full Power Bandwidth		22		MHz	At 3 dB
		5		MHz	At 0.1 dB

Parameter[1]	B Version Min	Typ	Max	Unit	Test Conditions/Comments
DC ACCURACY[4]					Single-ended/pseudo differential mode 1 LSB = FSR/4096, unless otherwise noted; differential mode 1 LSB = FSR/8192, unless otherwise noted
Resolution	13			Bits	
No Missing Codes	12-bit plus sign (13 bits)			Bits	Differential mode
	11-bit plus sign (12 bits)			Bits	Single-ended/pseudo differential mode
Integral Nonlinearity[2]			±1.25	LSB	Differential mode; V_{CC} = 3 V to 5.25 V, typical for V_{CC} = 2.7 V
			±1.2	LSB	Single-ended/pseudo differential mode, V_{CC} = 3 V to 5.25 V, typical for V_{CC} = 2.7 V
		−0.7/+1.2		LSB	Single-ended/pseudo differential mode (LSB = FSR/8192)
Differential Nonlinearity[2]			−0.99/+1.2	LSB	Differential mode; guaranteed no missing codes to 13 bits
			±0.99	LSB	Single-ended mode; guaranteed no missing codes to 12 bits
		−0.7/+1		LSB	Single-ended/pseudo differential mode (LSB = FSR/8192)
Offset Error[2, 5]			−6/+10	LSB	Single-ended/pseudo differential mode
			−7/+11	LSB	Differential mode
Offset Error Match[2, 5]			±0.8	LSB	Single-ended/pseudo differential mode
			±0.5	LSB	Differential mode
Gain Error[2, 5]			±8	LSB	Single-ended/pseudo differential mode
			±15	LSB	Differential mode
Gain Error Match[2, 5]			±0.5	LSB	Single-ended/pseudo differential mode
			±0.5	LSB	Differential mode
Positive Full-Scale Error[2, 6]			±4	LSB	Single-ended/pseudo differential mode
			±8	LSB	Differential mode
Positive Full-Scale Error Match[2, 6]			±0.5	LSB	Single-ended/pseudo differential mode
			±0.5	LSB	Differential mode
Bipolar Zero Error[2, 6]			±9	LSB	Single-ended/pseudo differential mode
			±8	LSB	Differential mode
Bipolar Zero Error Match[2, 6]			±0.5	LSB	Single-ended/pseudo differential mode
			±0.5	LSB	Differential mode
Negative Full-Scale Error[2, 6]			±4	LSB	Single-ended/pseudo differential mode
			±7	LSB	Differential mode
Negative Full-Scale Error Match[2, 6]			±0.5	LSB	Single-ended/pseudo differential mode
			±0.5	LSB	Differential mode
ANALOG INPUT					
Input Voltage Ranges[2]					Reference = 2.5 V
(Programmed via Range Registers)		±10		V	V_{DD} = +10 V min, V_{SS} = −10 V min, V_{CC} = +2.7 V to +5.25 V
		±5		V	V_{DD} = +5 V min, V_{SS} = −5 V min, V_{CC} = +2.7 V to +5.25 V
		±2.5		V	V_{DD} = +5 V min, V_{SS} = −5 V min, V_{CC} = +2.7 V to +5.25 V
		0 to 10		V	V_{DD} = +10 V min, V_{SS} = AGND min, V_{CC} = +2.7 V to +5.25 V

Parameter[1]	B Version Min	Typ	Max	Unit	Test Conditions/Comments
Pseudo Differential $V_{IN}(-)$ Input Range[2]					V_{DD} = +16.5 V, V_{SS} = −16.5 V, V_{CC} = +5 V
		±3.5		V	Reference = 2.5 V; range = ±10 V
		±6		V	Reference = 2.5 V; range = ±5 V
		±5		V	Reference = 2.5 V; range = ±2.5 V
		+3/−5		V	Reference = 2.5 V; range = 0 V to +10 V
DC Leakage Current			±80	nA	$V_{IN} = V_{DD}$ or V_{SS}
		3		nA	Per input channel, $V_{IN} = V_{DD}$ or V_{SS}
Input Capacitance[3]		13.5		pF	When in track, ±10 V range
		16.5		pF	When in track, ±5 V and 0 V to +10 V ranges
		21.5		pF	When in track, ±2.5 V range
		3		pF	When in hold, all ranges
REFERENCE INPUT/OUTPUT					
Input Voltage Range	2.5		3	V	
Input DC Leakage Current			±1	µA	
Input Capacitance		10		pF	
Reference Output Voltage		2.5		V	
Reference Output Voltage Error at 25°C			±5	mV	
Reference Output Voltage T_{MIN} to T_{MAX}			±10	mV	
Reference Temperature Coefficient			25	ppm/°C	
		3		ppm/°C	
Reference Output Impedance		7		Ω	
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4			V	
Input Low Voltage, V_{INL}			0.8	V	V_{CC} = 4.75 V to 5.25 V
			0.4	V	V_{CC} = 2.7 to 3.6 V
Input Current, I_{IN}			±1	µA	V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[3]		10		pF	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	V_{DRIVE} − 0.2 V			V	I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 200 µA
Floating-State Leakage Current			±1	µA	
Floating-State Output Capacitance[3]		5		pF	
Output Coding		Straight natural binary			Coding bit set to 1 in control register
		Twos complement			Coding bit set to 0 in control register
CONVERSION RATE					
Conversion Time			1.6	µs	16 SCLK cycles with SCLK = 10 MHz
Track-and-Hold Acquisition Time[2, 3]			305	ns	Full-scale step input
Throughput Rate			500	kSPS	
POWER REQUIREMENTS					Digital inputs = 0 V or V_{DRIVE}
V_{DD}[2]	12		16.5	V	
V_{SS}[2]	−12		−16.5	V	
V_{CC}[2]	2.7		5.25	V	
V_{DRIVE}	2.7		5.25	V	
Normal Mode (Static)		0.9		mA	V_{DD}/V_{SS} = ±16.5 V, V_{CC}/V_{DRIVE} = 5.25 V

Parameter[1]	B Version Min	Typ	Max	Unit	Test Conditions/Comments
Normal Mode (Operational)					f_{SAMPLE} = 500 kSPS
I_{DD}			195	μA	V_{DD} = 16.5 V
I_{SS}			215	μA	V_{SS} = −16.5 V
I_{CC} and I_{DRIVE}			2.3	mA	V_{CC}/V_{DRIVE} = 5.25 V
Autostandby Mode (Dynamic)					f_{SAMPLE} = 250 kSPS
I_{DD}			100	μA	V_{DD} = 16.5 V
I_{SS}			110	μA	V_{SS} = −16.5 V
I_{CC} and I_{DRIVE}			0.87	mA	V_{CC}/V_{DRIVE} = 5.25 V
Autoshutdown Mode (Static)					SCLK on or off
I_{DD}			1	μA	V_{DD} = 16.5 V
I_{SS}			1	μA	V_{SS} = −16.5 V
I_{CC} and I_{DRIVE}			1	μA	V_{CC}/V_{DRIVE} = 5.25 V
Full Shutdown Mode					SCLK on or off
I_{DD}			1	μA	V_{DD} = 16.5 V
I_{SS}			1	μA	V_{SS} = −16.5 V
I_{CC} and I_{DRIVE}			1	μA	V_{CC}/V_{DRIVE} = 5.25 V
POWER DISSIPATION					
Normal Mode (Operational)			19	mW	V_{DD} = +16.5 V, V_{SS} = −16.5 V, V_{CC} = +5.25 V
Full Shutdown Mode			38.25	μW	V_{DD} = +16.5 V, V_{SS} = −16.5 V, V_{CC} = +5.25 V

[1] Temperature range is −55°C to +125°C.
[2] See the terminology section of the AD7327 data sheet.
[3] Sample tested during initial release to ensure compliance.
[4] For dc accuracy specifications, the LSB size for differential mode is FSR/8192. For single-ended mode/pseudo differential mode, the LSB size is FSR/4096, unless otherwise noted.
[5] Unipolar 0 V to 10 V range with straight binary output coding.
[6] Bipolar range with twos complement output coding.

TIMING SPECIFICATIONS

V_{DD} = 12 V to 16.5 V, V_{SS} = −12 V to −16.5 V, V_{CC} = 2.7 V to 5.25 V, V_{DRIVE} = 2.7 V to 5.25 V, V_{REF} = 2.5 V to 3.0 V internal/external, $T_A = T_{MAX}$ to T_{MIN}. Timing specifications apply with a 32 pF load, unless otherwise noted.[1]

Table 2.

	Limit at T_{MIN}, T_{MAX}			Description
Parameter	**V_{CC} < 4.75 V**	**V_{CC} = 4.75 V to 5.25 V**	**Unit**	**$V_{DRIVE} \le V_{CC}$**
f_{SCLK}	50	50	kHz min	
	10	10	MHz max	
$t_{CONVERT}$	16 × t_{SCLK}	16 × t_{SCLK}	ns max	$t_{SCLK} = 1/f_{SCLK}$
t_{QUIET}	75	60	ns min	Minimum time between end of serial read and next falling edge of $\overline{CS}$
t_1	12	5	ns min	Minimum $\overline{CS}$ pulse width
t_2[2]	25	20	ns min	$\overline{CS}$ to SCLK set-up time; bipolar input ranges (±10 V, ±5 V, ±2.5 V)
	45	35	ns min	Unipolar input range (0 V to 10 V)
t_3	26	14	ns max	Delay from $\overline{CS}$ until DOUT three-state disabled
t_4	57	43	ns max	Data access time after SCLK falling edge
t_5	0.4 × t_{SCLK}	0.4 × t_{SCLK}	ns min	SCLK low pulse width
t_6	0.4 × t_{SCLK}	0.4 × t_{SCLK}	ns min	SCLK high pulse width
t_7	13	8	ns min	SCLK to data valid hold time
t_8	40	22	ns max	SCLK falling edge to DOUT high impedance
	10	9	ns min	SCLK falling edge to DOUT high impedance
t_9	4	4	ns min	DIN set-up time prior to SCLK falling edge
t_{10}	2	2	ns min	DIN hold time after SCLK falling edge
$t_{POWER-UP}$	750	750	ns max	Power-up from autostandby
	500	500	µs max	Power-up from full shutdown/autoshutdown mode, internal reference
	25	25	µs typ	Power-up from full shutdown/autoshutdown mode, external reference

[1] Sample tested during initial release to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DRIVE}) and timed from a voltage level of 1.6 V.
[2] When using the 0 V to 10 V unipolar range, running at 500 kSPS throughput rate with t_2 at 20 ns, the mark space ratio needs to be limited to 50:50.

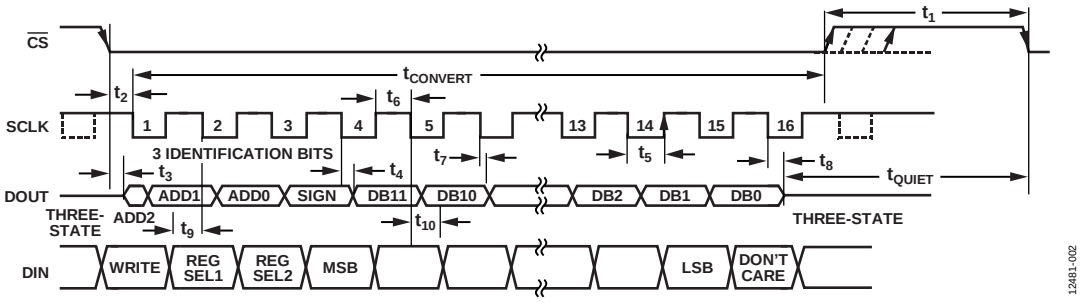

Figure 2. Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to AGND, DGND	−0.3 V to +16.5 V
V_{SS} to AGND, DGND	+0.3 V to −16.5 V
V_{DD} to V_{CC}	V_{CC} − 0.3 V to 16.5 V
V_{CC} to AGND, DGND	−0.3 V to +7 V
V_{DRIVE} to AGND, DGND	−0.3 V to +7 V
AGND to DGND	−0.3 V to +0.3 V
Analog Input Voltage to AGND	V_{SS} − 0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to +7 V
Digital Output Voltage to GND	−0.3 V to V_{DRIVE} + 0.3 V
REFIN to AGND	−0.3 V to V_{CC} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
TSSOP Package	
θ_{JA} Thermal Impedance	143°C/W
θ_{JC} Thermal Impedance	45°C/W
Pb-Free Temperature, Soldering Reflow	260(0)°C
ESD	2.5 kV

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

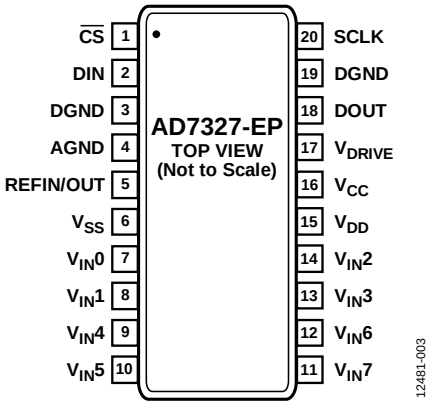

Figure 3. TSSOP Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7327-EP and frames the serial data transfer.
2	DIN	Data In. Data to be written to the on-chip registers is provided on this input and is clocked into the AD7327-EP on the falling edge of SCLK (see the Registers section of AD7327 data sheet).
3, 19	DGND	Digital Ground. Ground reference point for all digital circuitry on the AD7327-EP. The DGND and AGND voltages, ideally, share the same potential and must not be more than 0.3 V apart, even on a transient basis.
4	AGND	Analog Ground. Ground reference point for all analog circuitry on the AD7327-EP. Refer all analog input signals and any external reference signal to this AGND voltage. The AGND and DGND voltages, ideally, share the same potential and must not be more than 0.3 V apart, even on a transient basis.
5	REFIN/OUT	Reference Input/Reference Output. The on-chip reference is available on this pin for external use to the AD7327-EP. The nominal internal reference voltage is 2.5 V, which appears at this pin. Place a 680 nF capacitor on the reference pin (see the Reference section of the AD7327 data sheet). Alternatively, the internal reference can be disabled and an external reference applied to this input. On power-up, the external reference mode is the default condition.
6	V_{SS}	Negative Power Supply Voltage. This is the negative supply voltage for the analog input section.
7, 8, 14, 13, 9, 10, 12, 11	$V_{IN}0$ to $V_{IN}7$	Analog Input 0 to Analog Input 7. The analog inputs are multiplexed into the on-chip track-and-hold. The analog input channel for conversion is selected by programming the channel address Bit ADD2 through Bit ADD0 in the control register. The inputs can be configured as eight single-ended inputs, four true differential input pairs, four pseudo differential inputs, or seven pseudo differential inputs. The configuration of the analog inputs is selected by programming the mode bits, Bit Mode 1 and Bit Mode 0, in the control register. The input range on each input channel is controlled by programming the range registers. Input ranges of ±10 V, ±5 V, ±2.5 V, and 0 V to +10 V can be selected on each analog input channel when a +2.5 V reference voltage is used (see the Registers section of AD7327 data sheet).
15	V_{DD}	Positive Power Supply Voltage. This is the positive supply voltage for the analog input section.
16	V_{CC}	Analog Supply Voltage, 2.7 V to 5.25 V. This is the supply voltage for the ADC core on the AD7327-EP. Decouple this supply to AGND.
17	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the interface operates. Decouple this pin to DGND. The voltage at this pin may be different to that at V_{CC}, but it must not exceed V_{CC} by more than 0.3 V.
18	DOUT	Serial Data Output. The conversion output data is supplied to this pin as a serial data stream. The bits are clocked out on the falling edge of the SCLK input, and 16 SCLKs are required to access the data. The data stream consists of three channel identification bits, the sign bit, and 12 bits of conversion data. The data is provided MSB first (see the Serial Interface section of AD7327 data sheet).
20	SCLK	Serial Clock, Logic Input. A serial clock input provides the SCLK used for accessing the data from the AD7327-EP. This clock is also used as the clock source for the conversion process.

TYPICAL PERFORMANCE CHARACTERISTICS

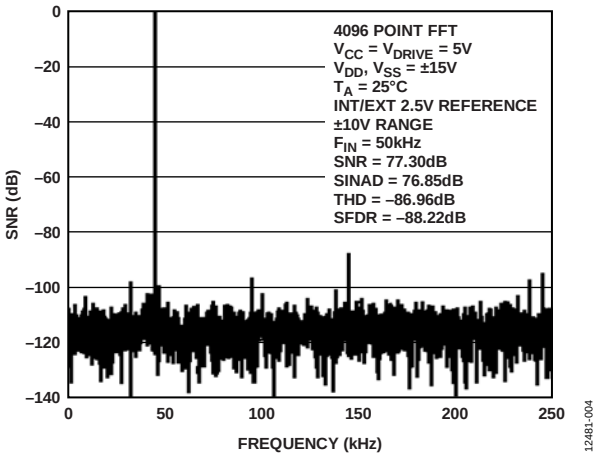

Figure 4. FFT True Differential Mode

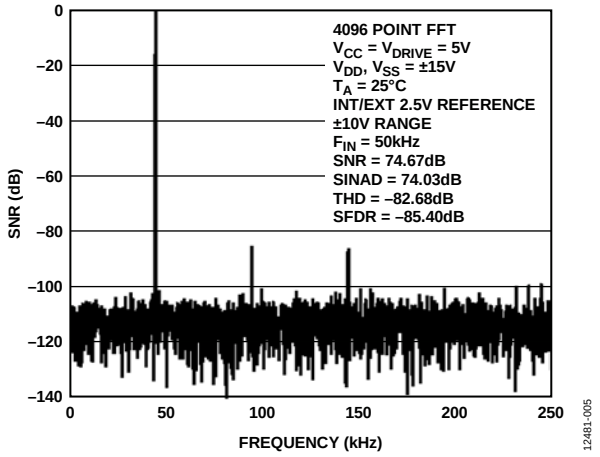

Figure 5. FFT Single-Ended Mode

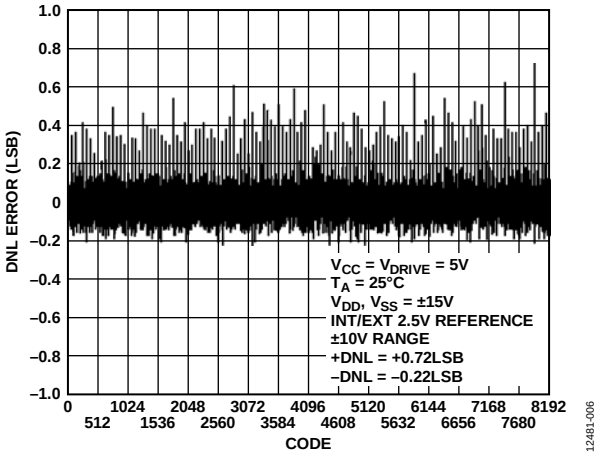

Figure 6. Typical DNL True Differential Mode

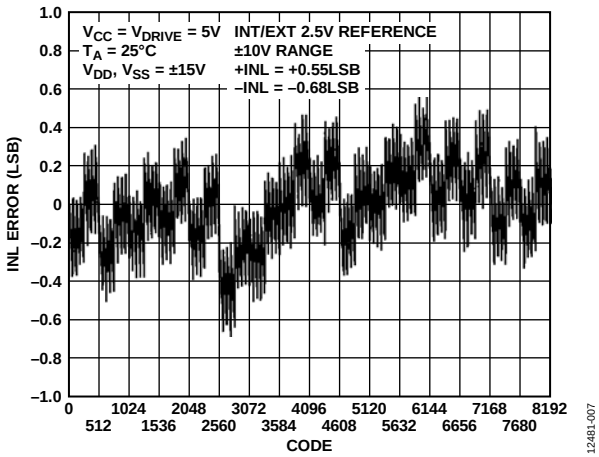

Figure 7. Typical INL True Differential Mode

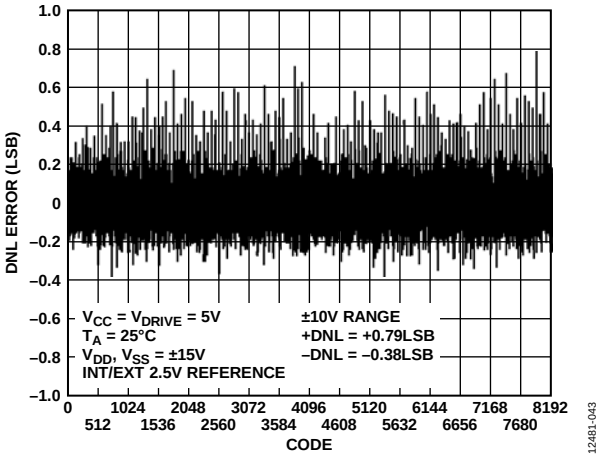

Figure 8. Typical DNL Single-Ended Mode

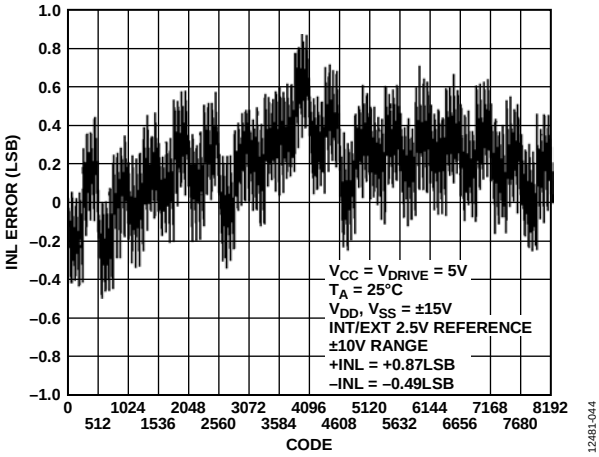

Figure 9. Typical INL Single-Ended Mode

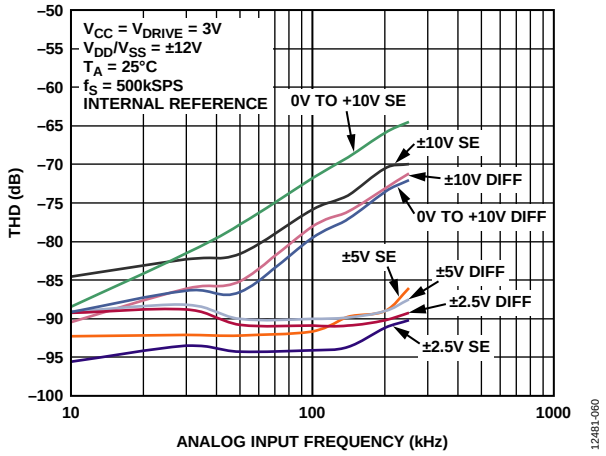

Figure 10. THD vs. Analog Input Frequency for Single-Ended (SE) and True Differential Mode (Diff) at 3 V V_{CC}

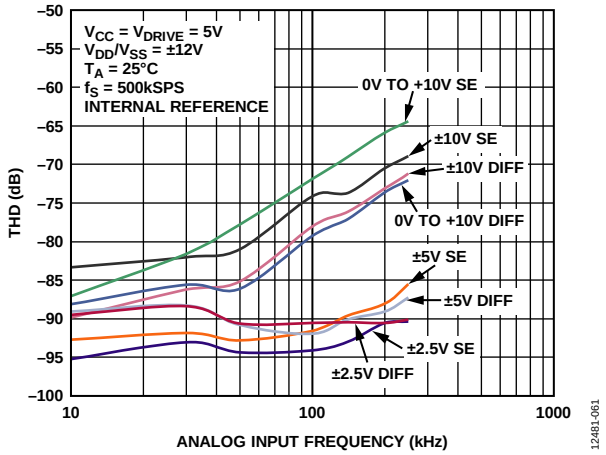

Figure 11. THD vs. Analog Input Frequency for Single-Ended (SE) and True Differential Mode (Diff) at 5 V V_{CC}

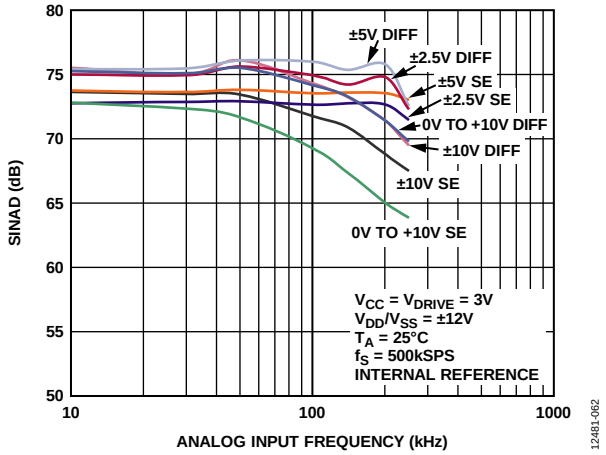

Figure 12. SINAD vs. Analog Input Frequency for Single-Ended (SE) and True Differential Mode (Diff) at 3 V V_{CC}

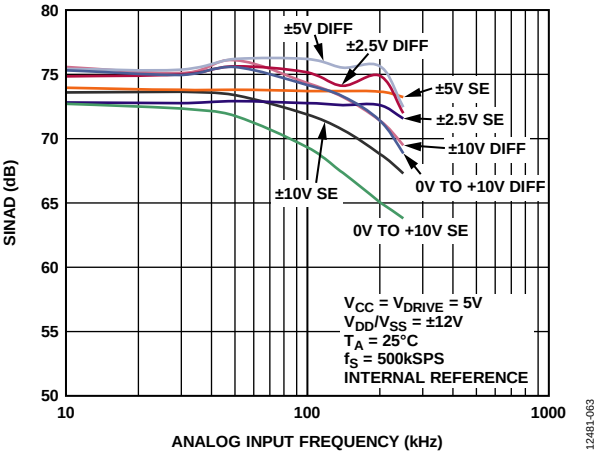

Figure 13. SINAD vs. Analog Input Frequency for Single-Ended (SE) and True Differential Mode (Diff) at 5 V V_{CC}

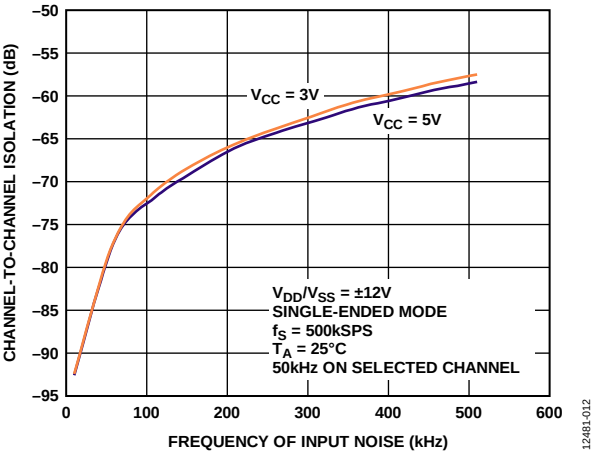

Figure 14. Channel-to-Channel Isolation

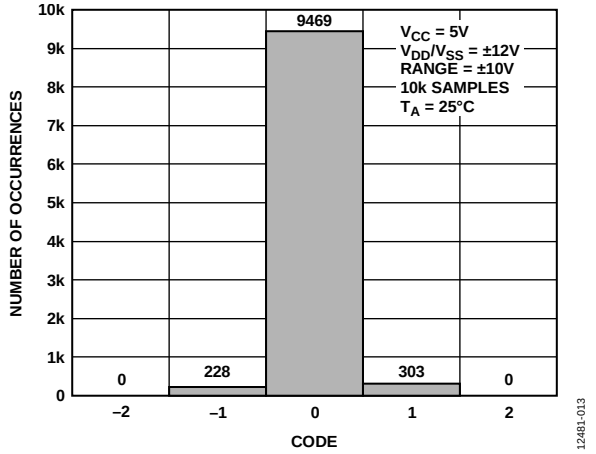

Figure 15. Histogram of Codes, True Differential Mode

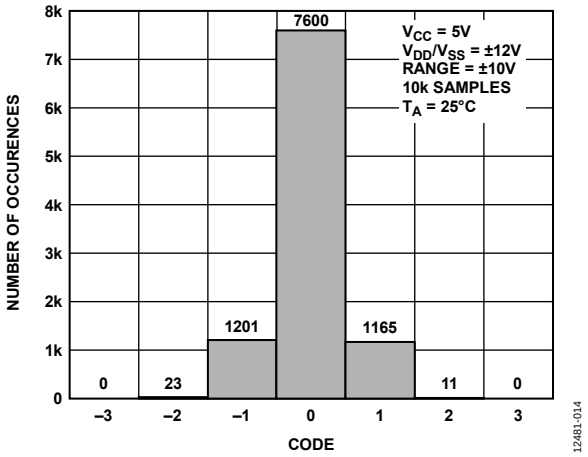

Figure 16. Histogram of Codes, Single-Ended Mode

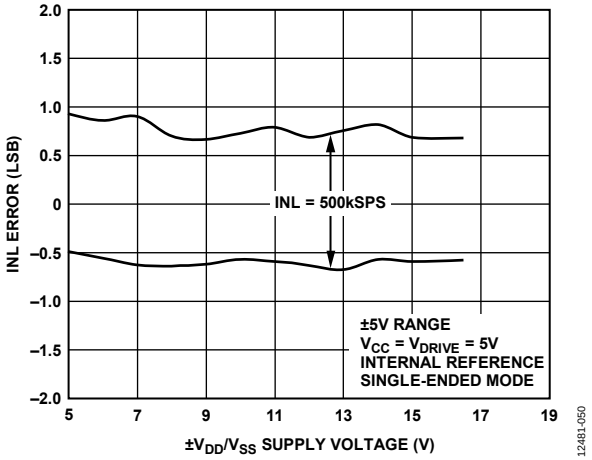

Figure 19. INL Error vs. Supply Voltage at 500 kSPS

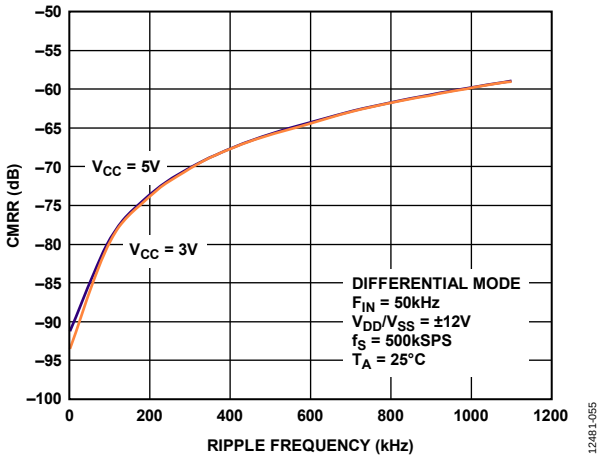

Figure 17. CMRR vs. Common-Mode Ripple Frequency

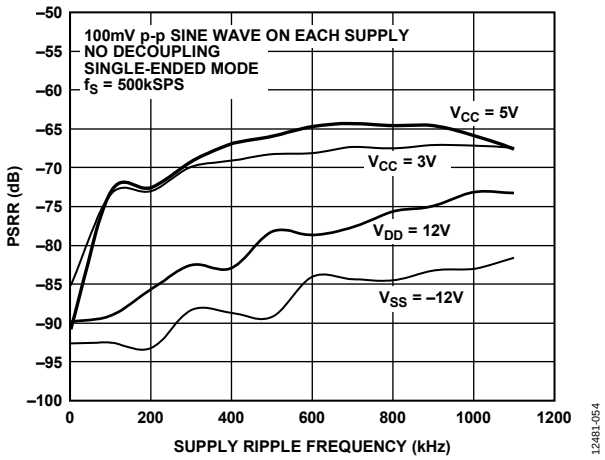

Figure 20. PSRR vs. Supply Ripple Frequency Without Supply Decoupling

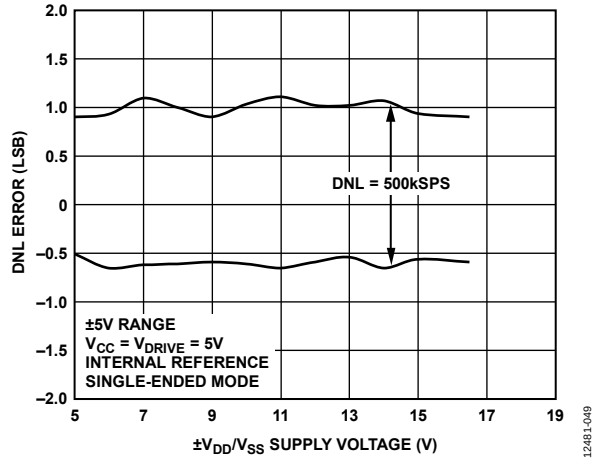

Figure 18. DNL Error vs. Supply Voltage at 500 kSPS

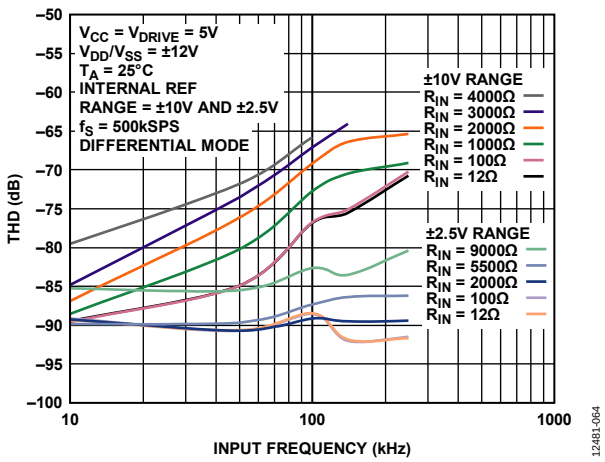

Figure 21. THD vs. Analog Input Frequency for Various Source Impedances, True Differential Mode

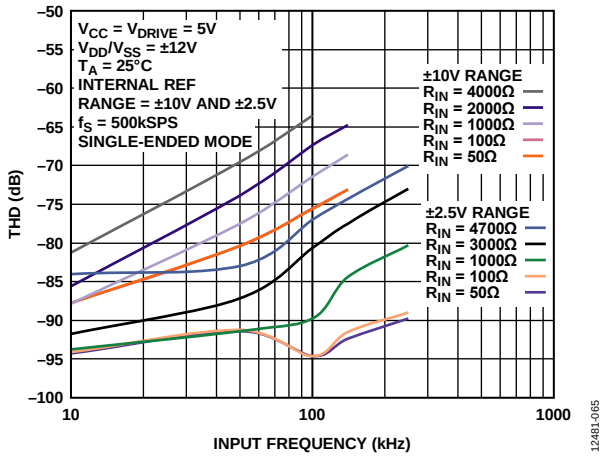

Figure 22. THD vs. Analog Input Frequency for Various Source Impedances, Single-Ended Mode

OUTLINE DIMENSIONS

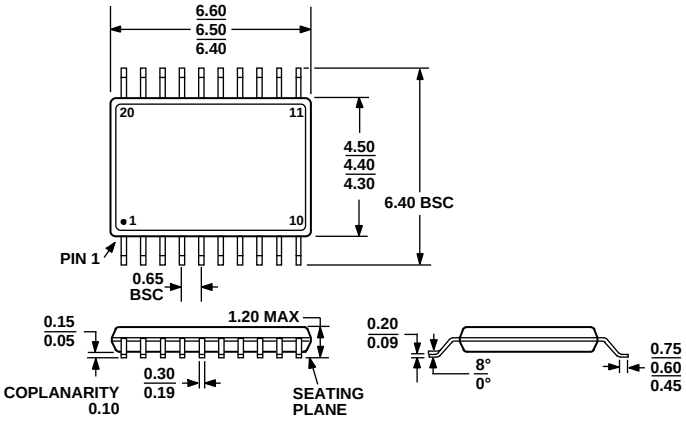

Figure 23. 20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions show in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD7327TRU-EP	−55°C to +125°C	20-Lead [TSSOP]	RU-20
AD7327TRU-EP-RL7	−55°C to +125°C	20-Lead [TSSOP]	RU-20
EVAL-AD7327SDZ		Evaluation Board	
EVAL-SDP-CB1Z		Controller Board	

[1] Z = RoHS Compliant Part

D12481-0-9/15(B)