Data Sheet December 2, 2005 FN9248.0

Precision Multi-Phase Buck PWM Controller

The ISL9500 multi-phase Buck PWM control IC, with integrated half bridge gate drivers, provides a precision voltage regulation system for microprocessors in notebook computers. Two-phase operation eases the thermal management issues and load demand of high performance processors. This control IC also features both input voltage feed-forward and average current mode control for excellent dynamic response, “Loss-less” current sensing using MOSFET $r_{DS(ON)}$ and user selectable switching frequencies from 250kHz to 1MHz per phase.

The ISL9500 includes a 6-bit digital-to-analog converter (DAC) that dynamically adjusts the CORE PWM output voltage. The ISL9500 also has logic inputs to select Active, Deep Sleep and Deeper Sleep modes of operation. A precision reference, remote sensing and proprietary architecture, with integrated, processor-mode, compensated “Droop”, provide excellent static and dynamic CORE voltage regulation.

To improve efficiency at light loading, the ISL9500 can be configured to run in single phase PWM in Active, Deep or Deeper Sleep modes of operation. Also, in Deep and Deeper sleep modes the ISL9500 will operate in diode emulation.

Another feature of this IC controller is the PGOOD monitor circuit that is held low until CORE voltage increases, during its soft-start sequence, to within 12% of the “Boot” voltage. This PGOOD signal is masked during VID changes. Output overcurrent, overvoltage and undervoltage are monitored and result in the converter latching off and PGOOD signal being held low.

The overvoltage and undervoltage thresholds are 112% and 84% of the VID, Deep or Deeper Sleep setpoint, respectively. Overcurrent protection features a 32 cycle overcurrent shutdown. PGOOD, overvoltage, undervoltage and overcurrent provide monitoring and protection for the microprocessor and power system. The ISL9500 IC is available in a 38 lead TSSOP.

Features

- Diode Emulation Functionality in Deep and Deeper Sleep Modes for Improved Light Load Efficiency
- Single and/or Two-phase Power Conversion
- “Loss-less” Current sensing for Improved Efficiency and Reduced Board Area
  - Optional Discrete Precision Current Sense Resistor
- Internal Gate-Drive and Boot-Strap Diodes
- Precision CORE Voltage Regulation
  - 0.8% System Accuracy Over Temperature
- 6-Bit Microprocessor Voltage Identification Input
- Programmable “Droop” and CORE Voltage Slew Rate
- Direct Interface with System Logic for Deep and Deeper Sleep modes of operation
- Easily Programmable Voltage Setpoints for Initial “Boot”, Deep Sleep and Deeper Sleep Modes
- Excellent Dynamic Response
  - Combined Voltage Feed-Forward and Average Current Mode Control
- Overvoltage, Undervoltage and Overcurrent Protection
- Power-Good Output with Internal Blanking during VID and Mode Changes
- User programmable Switching Frequency of 250kHz - 1MHz
- Pb-Free Plus Anneal Available (RoHS Compliant)

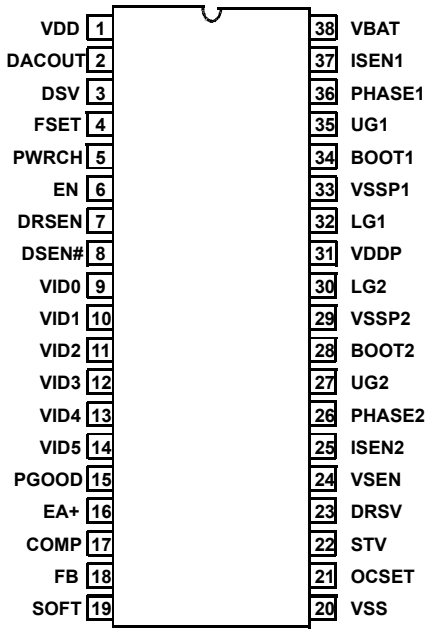
Ordering Information

PART NUMBER	PART MARKING	TEMP RANGE (°C)	PACKAGE	PKG. DWG. #
ISL9500CVZ (See Note)	ISL9500CVZ	-10 to 85	38 Ld TSSOP (Pb-free)	M38.173
ISL9500CVZ-T (See Note)	ISL9500CVZ	-10 to 85	38 Ld TSSOP Tape and Reel (Pb-free)	M38.173

NOTE:
Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout

ISL9500 (38 LD TSSOP)
TOP VIEW



Absolute Voltage Ratings

Supply Voltage, VDD, VDDP . . . . . -0.3-+7V
Battery Voltage, VBAT . . . . . +25V
Boot1, 2 and UGATE1, 2 . . . . . +35V
Phase1, 2 and ISEN1, 2 . . . . . +30V
Boot1, 2 with Respect to Phase1, 2. . . . . +6.5V
UGATE1,2 . . . . . .(Phase1, 2 - 0.3V) to (Boot1,2 + 0.3V)
All Other Pins. . . . . -0.3V to (VDD + 0.3V)

Recommended Operating Conditions

Supply Voltage, VDD, VDDP . . . . . +5V ±5%
Ambient Temperature. . . . . .-10°C to 85°C
Junction Temperature . . . . . .-10°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
TSSOP Package (Note 1) 72
Maximum Operating Junction Temperature. . . . . 125°C
Maximum Storage Temperature Range. . . . . .-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

CAUTION: Stress above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air.

Electrical Specifications

V_{DD} = 5V, T_A = -10° to 85°C, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT POWER SUPPLY					
Input Supply Current, I(VDD)	EN = 3.3V, DSEN# = 0, DRSEN = 0, PWRCH = 0	-	1.4	-	mA
	EN = 0V	-	1	-	µA
POR (Power-On Reset) Threshold	V_{DD} Rising	4.35	4.45	4.5	V
	V_{DD} Falling	4.05	4.20	4.40	V
REFERENCE AND DAC					
System Accuracy	Percent system deviation from programmed VID Codes @ 1.356	-0.8	-	0.8	%
DAC (VID0 - VID5) Input Low Voltage	DAC Programming Input Low Threshold Voltage	-	-	0.3	V
DAC (VID0 - VID5) Input High Voltage	DAC Programming Input High Threshold Voltage	0.7	-	-	V
Maximum Output Voltage (VID = 000000)		-	1.708	-	V
Minimum Output Voltage (VID = 111111)		-	0.70	-	V
CHANNEL GENERATOR					
Frequency, F_{SW}	R_{Fset} = 243K, ±1%	225	250	275	kHz
Adjustment Range	Guaranteed by Design	0.25	-	1.0	MHz
ERROR AMPLIFIER					
DC Gain		-	100	-	dB
Gain-Bandwidth Product	C_L = 20pF	-	18	-	MHz
Slew Rate	C_L = 20pF	-	4.0	-	V/µs
ISEN					
Full Scale Input Current		-	32	-	µA
Overcurrent Threshold	R_{OCSET} = 124K	-	64	-	µA
Soft-Start Current		-	31	-	µA
Droop Current		27	28.5	30	µA
GATE DRIVER					
UGATE Source Resistance	500mA Source Current	-	1	1.5	Ω

Electrical Specifications V_{DD} = 5V, T_A = -10° to 85°C, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UGATE Source Current	$V_{UGATE-PHASE}$ = 2.5V	-	2	-	A
UGATE Sink Resistance	500mA Sink Current	-	1	1.5	Ω
UGATE Sink Current	$V_{UGATE-PHASE}$ = 2.5V	-	2	-	A
LGATE Source Resistance	500mA Source Current	-	1	1.5	Ω
LGATE Source Current	V_{LGATE} = 2.5V	-	2	-	A
LGATE Sink Resistance	500mA Sink Current	-	0.5	0.8	Ω
LGATE Sink Current	V_{LGATE} = 2.5V	-	4	-	A
BOOTSTRAP DIODE					
Forward Voltage	VDDP = 5V, Forward Bias Current = 10mA	0.58	0.68	0.76	V
POWER GOOD MONITOR					
PGOOD Sense Current		2.43	-	-	mA
PGOOD Pull Down MOSFET $r_{DS(ON)}$	(See Figure 10)	56	63	82	Ω
Undervoltage Threshold (Vsen/Vref)	VSEN Rising	-	85.0	-	%
Undervoltage Threshold (Vsen/Vref)	VSEN Falling	-	84.0	-	%
PGOOD Low Output Voltage	I_{PGOOD} = 4mA	-	0.26	0.4	V
LOGIC THRESHOLD					
EN, DSEN#, DRSEN Low		-	-	1	V
EN, DSEN#, DRSEN High		2	-	-	V
PROTECTION					
Overvoltage Threshold (Vsen/Vref)	VSEN Rising	-	112.0	-	%
DELAY TIME					
Delay Time from LGATE Falling to UGATE Rising	VDDP = 5V, BOOT to PHASE = 5V, UGATE – PHASE = 1V, LGATE = 1V	10	18	30	ns
Delay Time from UGATE Falling to LGATE Rising	VDDP = 5V, BOOT to PHASE = 5V, UGATE – PHASE = 1V, LGATE = 1V	10	18	30	ns

Functional Pin Description

VDD - This pin is used to connect +5V to the IC to supply all power necessary to operate the chip. The IC starts to operate when the voltage on this pin exceeds the rising POR threshold and shuts down when the voltage on this pin drops below the falling POR threshold.

DACOUT - This pin provides access to the output of the Digital-to-Analog converter.

DSV - The voltage on this pin provides the set point for output voltage during Deep Sleep mode of operation.

FSET - A resistor from this pin to ground programs the switching frequency.

PWRCH - This pin selects the number of power channels. A HIGH logic level on this pin enables 2 channel operation, and a LOW logic signal enables single channel operation.

EN - This pin is connected to the system signal VR_ON and provides the enable/disable function for the PWM controller.

DRSEN - This pin enables Deeper Sleep mode of operation when a logic HIGH is detected on this pin.

DSEN# - This pin enables Deep Sleep mode of operation when a logic LOW signal is detected on this pin.

VID0, VID1, VID2, VID3, VID4, VID5 - These pins are used as inputs to the 6-bit Digital-to-Analog converter (DAC). VID0 is the least significant bit and VID5 is the most significant bit. The VID step size is 16mV.

PGOOD - This pin is used as an input and an output, and is tied to the Vccp and Vcc_mch PGOOD signals. During start-up, this pin is recognized as an input and prevents further slewing of the output voltage from the “Boot” level until PGOOD from Vccp and Vcc_mch is enabled High. After start-up, this pin has an open drain output used to indicate the status of the CORE output voltage. This pin is pulled low when the system output is outside of the regulation limits. PGOOD includes a timer for power-on delay.

EA+ - This pin is connected to the non-inverting input of the error amplifier and is used for setting the “Droop” voltage.

COMP - This pin provides connection to the error amplifier output.

FB - This pin is connected to the inverting input of the error amplifier.

SOFT - This pin programs the slew rate of VID changes, Deep Sleep and Deeper Sleep transitions and soft-start after initializing. This pin is connected to ground via a capacitor, and to EA+ through an external “Droop” resistor.

VBAT - Voltage on this pin provides feed-forward battery information which adjusts the oscillator ramp amplitude.

ISEN1, ISEN2 - These pins are used as current sense inputs from the individual converter channel phase nodes.

PHASE1, PHASE2 - These pins are connected to the phase nodes of channels 1 and 2, respectively.

UG1, UG2 - These pins are the gate-drive outputs to the high side MOSFETs for channels 1 and 2, respectively.

BOOT1, BOOT2 - These pins are connected to the bootstrap capacitors, for upper gate-drive, for channels 1 and 2, respectively.

VSSP1, VSSP2 - These pins are connected to the power ground of channels 1 and 2, respectively.

LG1, LG2 - These pins are the gate-drive outputs to the low side MOSFETs for channels 1 and 2, respectively.

VDDP - This pin provides a low-ESR bypass connection to the internal gate drivers for the +5V source.

VSEN - This pin is used for remote sensing of the microprocessor CORE voltage.

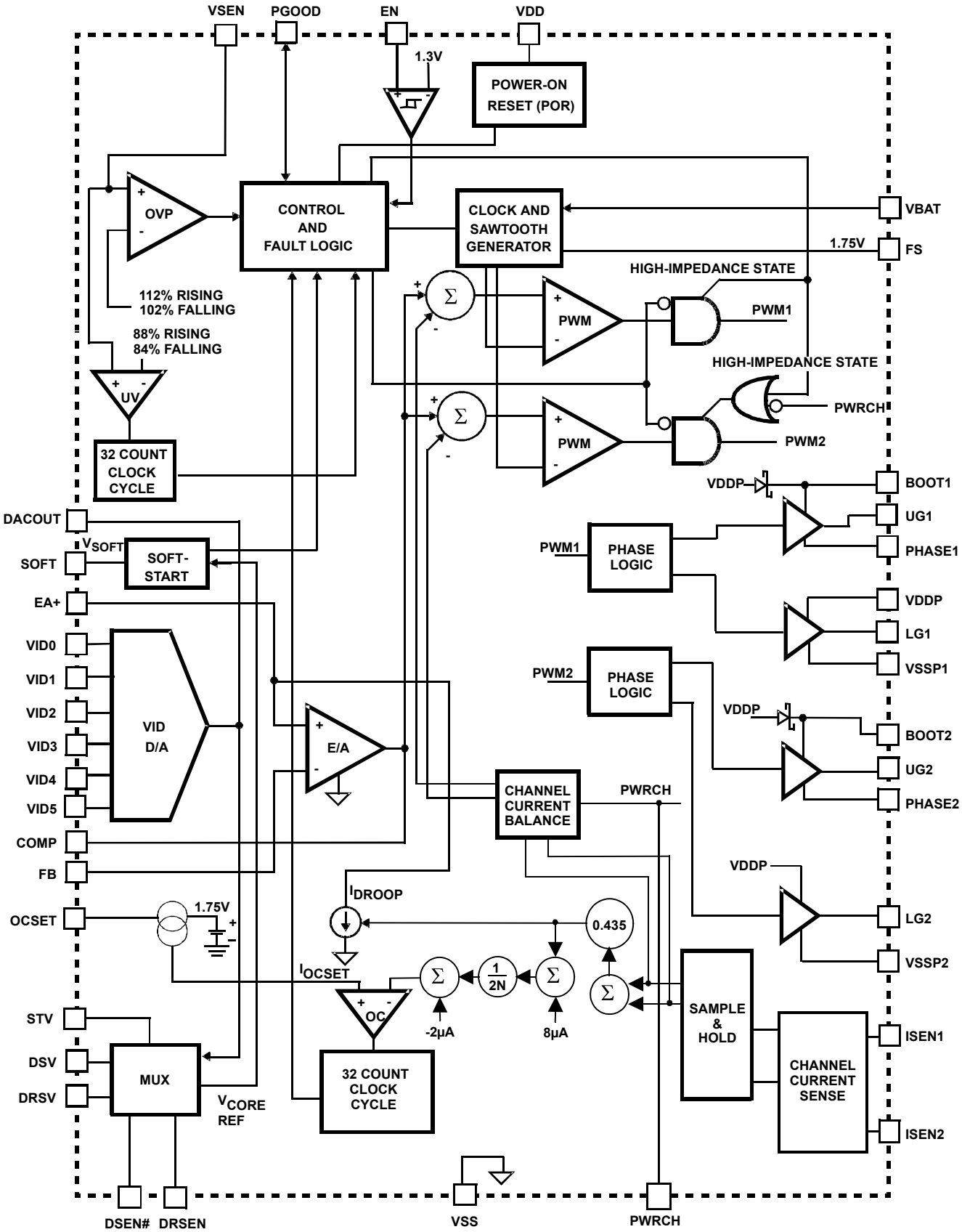
DRSV - The voltage on this pin provides the set point for output voltage during Deeper Sleep mode of operation.

OCSET - A resistor from this pin to ground sets the overcurrent protection threshold. The current from this pin should be between 10µA and 25µA (70kΩ - 175kΩ equivalent) pull-down resistance.

STV - The voltage on this pin sets the initial start-up or “Boot” voltage.

VSS - This pin provides connection for signal ground.

Block Diagram



Typical Application - 2-Phase Converter

Figure 1 shows a 2-Phase Synchronous Buck Converter circuit used to provide “CORE” voltage regulation.

The ISL9500 PWM controller can be configured for two or one channel operation, and the ISL9500 can change the number of power channels in operation, dynamically. The number of channels of operation can be changed through the PWRCH pin. The ISL9500 can be configured for two channel operation in “Active” mode and one channel operation in “Deep” and “Deeper Sleep” modes through logic connections to the PWRCH pin. The following configuration uses two channel operation in “Active” mode and one channel operation in “Deep” and “Deeper Sleep” modes.

The circuit shows pin connections for the ISL9500 PWM controller in the 38 lead TSSOP package.

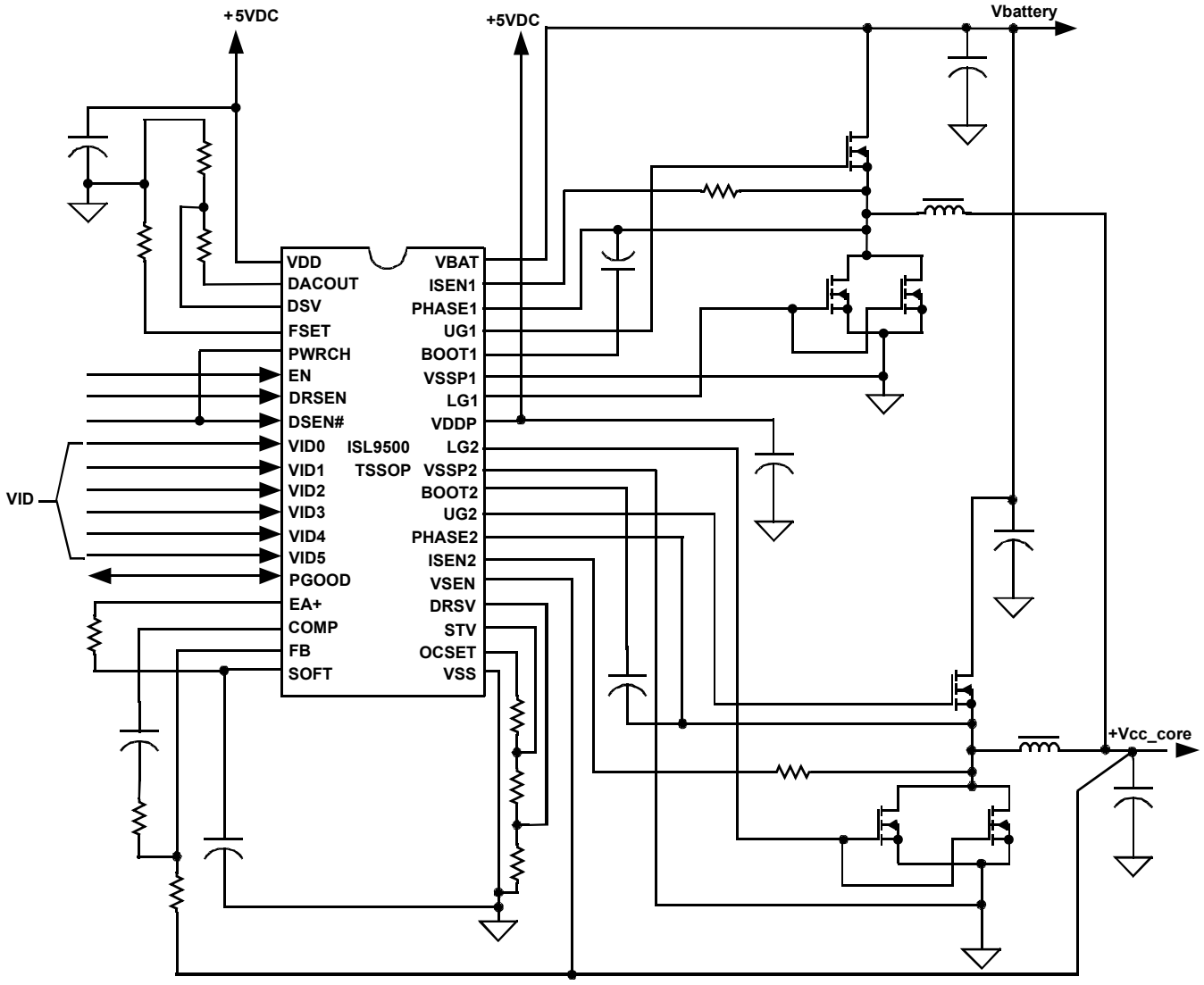


FIGURE 1. TYPICAL APPLICATION CIRCUIT FOR ISL9500 MULTI-PHASE PWM CONTROLLER

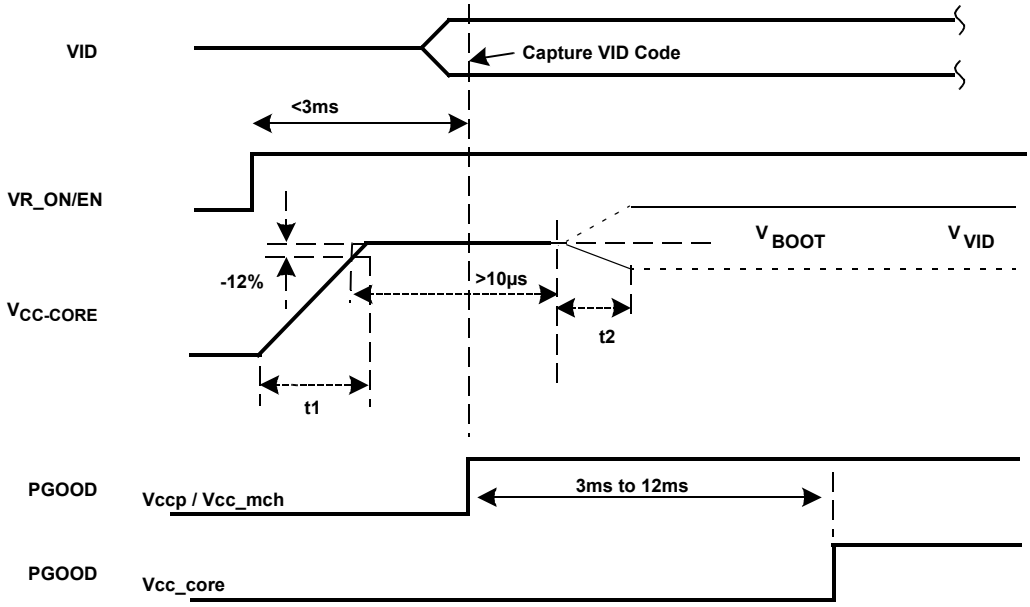


FIGURE 2. TIMING DIAGRAM SHOWING VR_ON, VCC_CORE AND PGOOD FOR VCC_CORE, VCCP AND VCC_MCH

Operation

Initialization

Once the +5VDC supply voltage, when connected to the ISL9500 VDD pin, reaches the Power-On Reset (POR) rising threshold, the PWM drive signals are held in “high-impedance state” or high impedance mode. This results in both high and low side MOSFETs being held low. Once the supply voltage exceeds the POR rising threshold, the controller will respond to a logic level high on the EN pin and initiate the soft-start interval. If the supply voltage drops below the POR falling threshold, POR shutdown is triggered and the PWM signals are again driven to “high-impedance state”.

The system signal, VR_ON is directly connected to the EN pin of the ISL9500. Once the voltage on the EN pin rises above 2.0V, the chip is enabled and soft-start begins. The EN pin of the ISL9500 is also used to reset the ISL9500, for cases when an undervoltage or overcurrent fault condition has latched the IC off. A toggling of the state of this pin to a level below 1.0V will re-enable the IC. For the case of an overvoltage fault, the VDD pin must be reset.

During start-up, the ISL9500 regulates to the voltage on the STV pin. This is referred to as the “Boot” voltage and is labelled VBOOT in Figure 2. Once power good signals are received from the Vccp and Vcc_mch regulators, the ISL9500 will capture the VID code and regulate to this command voltage within 3ms to 12ms. The PGOOD pin of the ISL9500 is both an input and an output and is further described in the “Fault Protection” section of this document.

Soft-Start Interval

Once VDD rises above the POR rising threshold and the EN pin voltage is above the threshold of 2.0V, a soft-start interval is initiated. Refer to Figure 2 and Figure 3.

The voltage on the EA+ pin is the reference voltage for the regulator. The voltage on the EA+ pin is equal to the voltage on the SOFT pin minus the “Droop” resistor voltage, VDROOP. During start-up, when the voltage on SOFT is less than the “Boot” voltage VBOOT, a small 30µA current source, I1, is used to slowly ramp up the voltage on the soft-start capacitor CSOFT. This slowly ramps up the reference voltage for the controller, and therefore, controls the slew rate of the output voltage. The STV pin is externally programmable and sets the start-up, or “Boot” voltage, VBOOT. The programming of this voltage level is explained in the “STV, DSV and DRSV” section of this document.

The ISL9500 PGOOD pin is both an input and an output. The system signal power good signal is connected to power good signals from the Vccp and Vcc_mch supplies. The Intersil ISL6227, Dual Voltage Regulator, is an ideal choice for the Vccp and Vcc_mch supplies.

Once the output voltage is within the “Boot” level regulation limits and a logic high PGOOD signal from the Vccp and Vccp_mch regulators is received, the ISL9500 is enabled to capture the VID code and regulate to that command voltage. Refer to Figure 2 and Figure 3. A second current source, I2, is added to I1, after the initial start-up transition. I2 is approximately 100µA, and raises the total SOFT pin sinking and sourcing current to 130µA. This increased current is used to increase the slew rate of the reference.

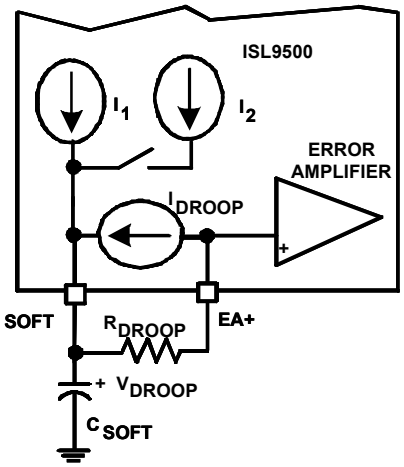


FIGURE 3. SOFT-START TRACKING CIRCUITRY SHOWING INTERNAL CURRENT SOURCES AND "DROOP" FOR ACTIVE, DEEP AND DEEPER SLEEP MODES OF OPERATION

The “Droop” current source, IDROOP, is proportional to load current. This current source is used to reduce the reference voltage on EA+ by the voltage drop across the “Droop” resistor. A more in-depth explanation of “Droop”, and the sizing of this resistor, can be found in the “Droop Compensation” section of this document.

The choice of value for soft-start capacitor is determined by the maximum slew rate required for the application. An example calculation is shown below. Using the combined I1 and I2 current sources on the SOFT pin as 130µA, and the worst case slew rate of (10mV/µs), the SOFT capacitor is calculated as follows:

$$C_{SOFT} = \frac{I_{SOURCE}}{SlewRate} = 130\mu A \times \frac{1\mu s}{10mV} = 0.013\mu F \approx 0.012\mu F \qquad \text{(EQ. 1)}$$

Gate-Drive Signals

The ISL9500 provides internal gate-drive for a two channel, synchronous buck, core regulator. During two channel mode of operation, the PWM drive signals are switched 180° out of phase to reduce ripple current delivered from the DC rail and to the load.

The ISL9500 was designed with a 4A, low-side gate current sink ability, and a 2A low-side gate current source ability, to efficiently drive the latest, high-performance MOSFETs. This feature will provide the system designer with flexibility in MOSFET selection, as well as optimum efficiency during Active mode of operation.

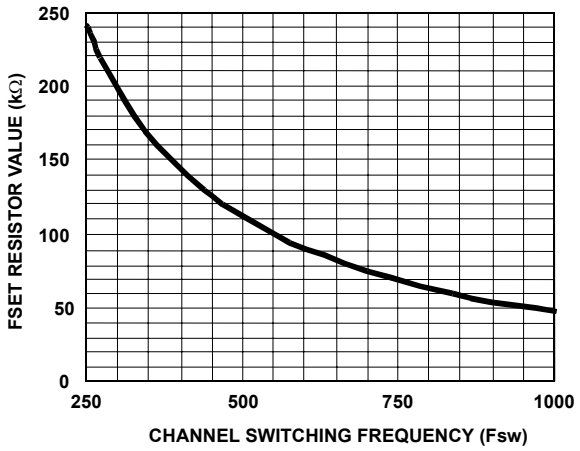


FIGURE 4. CHANNEL SWITCHING FREQUENCY vs R_{FSET}

PWRCH pin

A HIGH logic level on this pin enables two channel operation and a LOW logic signal enables single channel operation. By tying this pin to the DSEN# pin, single channel operation will be invoked during the light loading of both Deep and Deeper Sleep. If single channel operation is desired only during Deeper Sleep, the inversion of DRSEN can be connected to this pin.

The aggressive gate-drive capability and diode emulation of ISL9500, coupled with the single channel operation feature results in superior efficiency performance over both light and heavy loads.

Frequency Setting

Both channel switching frequencies are set up by a resistor from the FSET pin to ground. The choice of FSET resistance for a desired switching frequency can be approximated using Figure 4. The switching frequency is designed to operate between 250kHz and 1MHz per phase.

CORE Voltage Programming

The voltage identification pins (VID0, VID1, VID2, VID3, VID4 and VID5) set the DAC output voltage. These pins do not have internal pull-up or pull-down capability. These pins will recognize 1.0V, 3.3V or 5.0V CMOS logic.

The IC responds to VID code changes as shown in Figure 5. PGOOD is masked between these transitions.

Active, Deep Sleep and Deeper Sleep Modes

The ISL9500 multi-phase controller can operate in Active, Deep Sleep, and Deeper Sleep Modes.

After initial start-up, a logic high signal on DSEN# and a logic low signal on DRSEN signals the ISL9500 to operate in Active mode. Refer to Table 1. This mode will recognize VID code changes and regulate the output voltage to these command voltages.

TABLE 1. OUTPUT VOLTAGE AS A FUNCTION OF DSEN# AND DRSEN LOGIC STATES

DSEN# - STP_CPU#	DRSEN - DPRSLPVR	MODE OF OPERATION	OUTPUT VOLTAGE
1	0	Active	VID
0	0	Deep Sleep	DSV
0	1	Deeper Sleep	DRSV
1	1	Deeper Sleep	DRSV

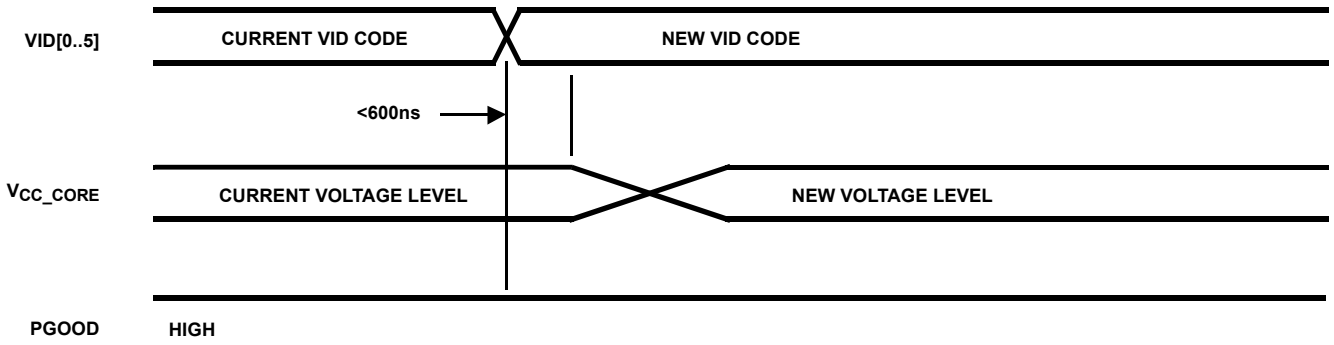


FIGURE 5. PLOT SHOWING TIMING OF VID CODE CHANGES AND CORE VOLTAGE SLEWING AS WELL AS PGOOD MASKING

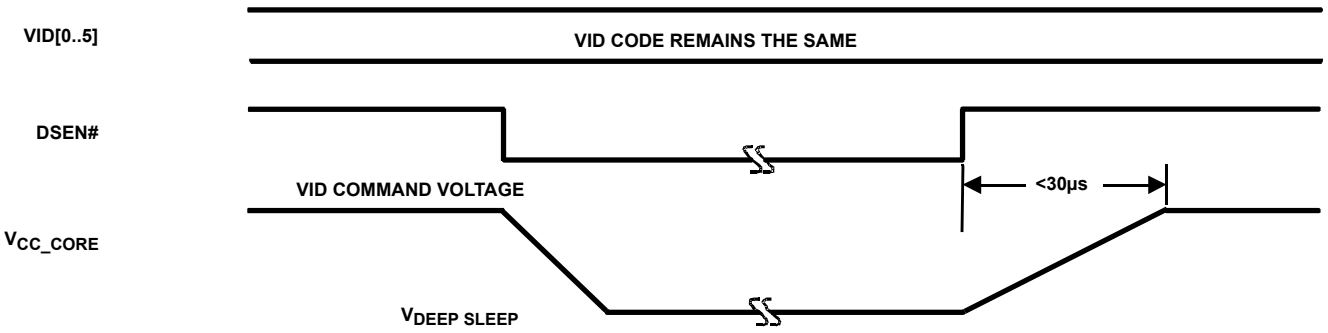


FIGURE 6. VCORE RESPONSE FOR DEEP SLEEP COMMAND

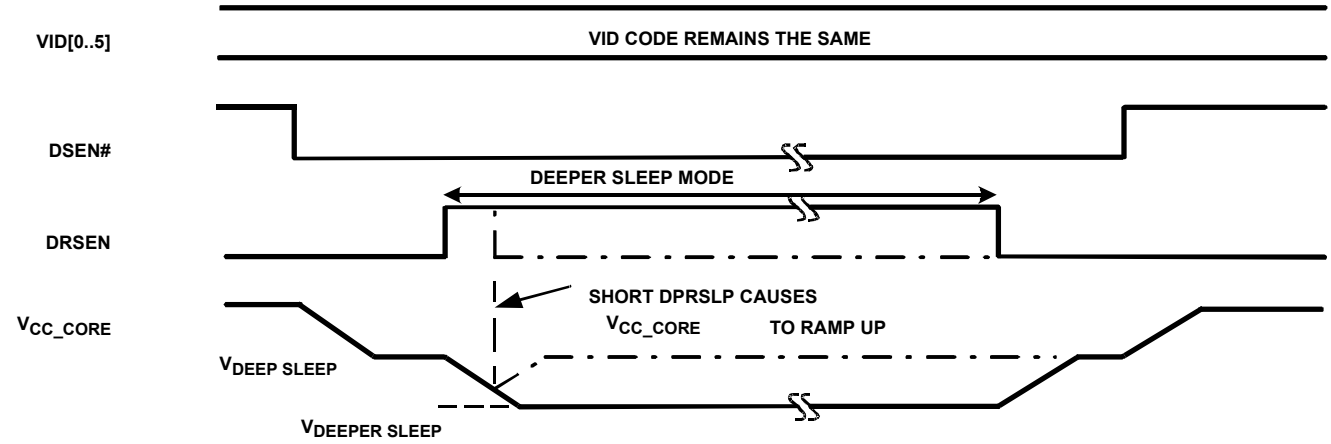


FIGURE 7. VCORE RESPONSE FOR DEEPER SLEEP COMMAND

A logic low signal present on DSEN#, with a logic low signal on DRSEN, signals the ISL9500 to reduce the CORE output voltage to the Deep Sleep level, the voltage on the DSV pin, and to operate in diode emulation.

A logic high on DRSEN with a logic low signal on DSEN#, signals the ISL9500 controller to further reduce the CORE output voltage to the Deeper Sleep level, which is the voltage on the DRSV pin.

Deep Sleep and Deeper Sleep voltage levels are programmable and are explained in the “STV, DSV and DRSV” section of this document.

Deep Sleep Enable-DSEN# and Deeper Sleep Enable - DRSEN

Table 1 shows logic states controlling modes of operation. Figure 6 and Figure 7 show the timing for transitions entering and exiting Deep Sleep Mode and Deeper Sleep Mode.

When DSEN# is logic high, and DRSEN is logic low, the controller will operate in Active Mode and regulate the output voltage to the VID commanded DAC voltage, minus the voltage “Droop” as determined by the load current. Voltage “Droop” is the reduction of output voltage proportional to output current.

When a logic low is detected at the DSEN# and DRSEN pins, the controller will regulate the output voltage to the voltage seen on the DSV pin minus “Droop”. If the PWRCH pin is connected to the DSEN# pin then the controller will also switch to single channel operation.

When DSEN# is logic low and DRSEN is logic high the controller will operate in Deeper Sleep mode. The ISL9500 will then regulate to the voltage at the DRSV pin minus “Droop”. If the PWRCH pin is connected to the DSEN# pin, then the controller will also automatically switch to single channel operation.

If the PWRCH pin is connected to an inverted DPRSLPVR system signal, then the controller will automatically switch to single channel operation during Deeper Sleep mode only. Deep and Deeper Sleep voltage levels are programmable and explained in the “STV, DSV and DRSV” section of this document.

STV, DSV and DRSV

Start-up “Boot” Voltage - STV

The start-up or “Boot” voltage is programmed by an external resistor divider network from the OCSET pin. Refer to Figure 8. Internally, a 1.75V reference voltage is output on the OCSET pin. The start-up voltage is set through a voltage divider from the 1.75V reference at the OCSET pin. The voltage on the STV pin will be the voltage the controller will regulate to during the start-up sequence.

Once the PGOOD pin of the ISL9500 controller is externally enabled high by the Vccp and Vcc_mch controllers, the ISL9500 will then ramp, after a 10µs delay, to the voltage commanded by the VID setting minus “Droop”.

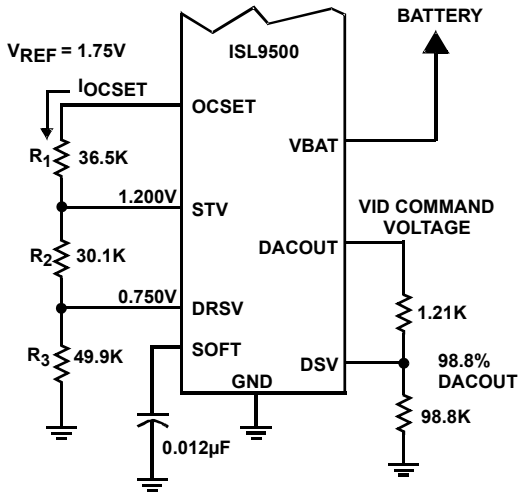


FIGURE 8. CONFIGURATIONS FOR BATTERY INPUT, OVERCURRENT SETTING AND START, DEEP SLEEP AND DEEPER SLEEP VOLTAGE DIVIDERS

Deep Sleep Voltage - DSV

The Deep Sleep voltage is programmed by an external voltage divider network from the DACOUT pin. Refer to Figure 8. The DACOUT pin is the output of the VID digital-to-analog converter. By having the Deep Sleep voltage set-up from a resistor divider from DAC, the Deep Sleep voltage will be a constant percentage of the VID. Through the voltage divider network, Deep Sleep voltage is set to 98.8% of the programmed VID voltage.

The IC enters the Deep Sleep mode when the DSEN# is low and the DRSEN pin is low as shown in Figure 6 and Figure 7. Once in Deep Sleep Mode, the controller will regulate to the voltage seen on the DSV pin minus “Droop”.

Deeper Sleep Voltage - DRSV

The Deeper Sleep voltage, DRSV, is programmed by an external voltage divider network from the 1.75V reference on the OCSET pin. Refer to Figure 8. In Deeper Sleep mode the ISL9500 controller will regulate the output voltage to the voltage present on the DRSV pin minus “Droop”. This voltage is easily changed by changing the ratio of R_1, R_2, and R_3.

The IC enters Deeper Sleep mode when DRSEN is high and DSEN# is low, as shown in Figure 7.

Overcurrent Setting - OCSET

The ISL9500 overcurrent protection essentially compares a user-selectable overcurrent threshold to the scaled and sampled output current. An overcurrent condition is defined when the sampled current is equal to or greater than the threshold current. A step by step process to design for the user-desired overcurrent set point is detailed next.

STEP 1: SETTING THE OVERCURRENT THRESHOLD

The overcurrent threshold is represented by the DC current flowing out of the OCSET pin (See Figure 8). Since the OCSET pin is held at a constant 1.75V, the user need only populate a resistor from this pin to ground to set the desired overcurrent threshold, I_{OCSET}. The user should pick a value of I_{OCSET} between 10µA and 25µA. Once this is done, use Ohm's Law to determine the necessary resistor to place from OCSET to ground

$$R_{OCSET} = \frac{1.75V}{I_{OCSET}} = R_1 + R_2 + R_3 \quad \text{(EQ. 2)}$$

For example, if the desired overcurrent threshold is 15µA, the total resistance from OCSET must equal 117kΩ.

STEP 2: SELECTING ISEN RESISTANCE FOR DESIRED OVERCURRENT LEVEL

After choosing the I_{OCSET} level, the user must then decide what level of total output current is desired for overcurrent. Typically, this number is between 150% and 200% of the maximum operating current of the application. For example, if the max operating current is 46A, and the user chooses 150% overcurrent, the ISL9500 will shut down if the output current exceeds 46A*1.5 or 69A. According to the Block Diagram, the equation below should be used to determine R_{ISEN} once the overcurrent level, I_{OC}, is chosen.

$$R_{ISEN} = \frac{I_{OC} \cdot \frac{r_{(DSON)}}{M} \cdot 0.2175}{(I_{OCSET} + 2\mu A) \cdot N - 4\mu A} - 130 \quad \text{(EQ. 3)}$$

In Equation 3, M represents the number of Low-Side MOSFETs in one channel, and N represents the number of channels. Using the examples above (I_{OC} = 69A, I_{OCSET} = 15µA) and substituting the values M = 2, N = 2, $r_{DS(ON)}$ = 6mΩ, R_{ISEN} is calculated to be 1.5kΩ.

STEP 3: THERMAL COMPENSATION FOR $R_{DS(ON)}$ (IF DESIRED)

If PTCs are used for thermal compensation, then R_{ISEN} is found using the room temperature value of $r_{DS(ON)}$. If standard resistors are used for RISEN, then the "HOT" value of $r_{DS(ON)}$ should be used for this calculation.

MOSFET $r_{DS(ON)}$ sensing provides advantages in cost, efficiency, and board area. However, if more precise current feedback is desired, a discrete Precision Current Sense Resistor, R_{POWER}, may be inserted between the SOURCE of each channels lower MOSFET and ground. The small R_{ISEN} resistor, as described above, is then replaced with a standard 1% resistor and connected from the ISEN pin of the ISL9500 controller to the SOURCE of the lower MOSFET.

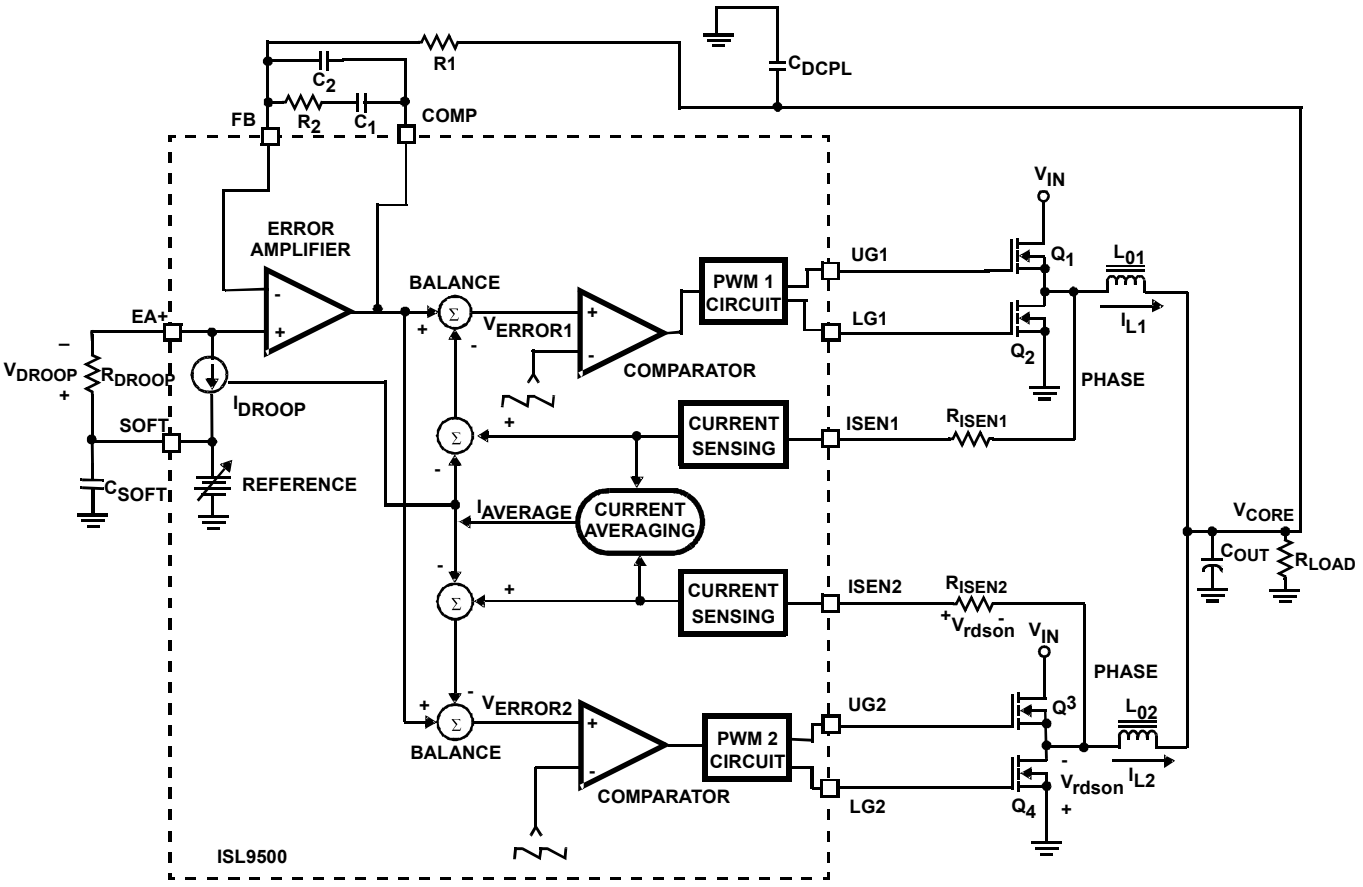


FIGURE 9. SIMPLIFIED BLOCK DIAGRAM OF THE ISL9500 VOLTAGE AND CURRENT CONTROL LOOPS FOR A TWO CHANNEL REGULATOR.

Battery Feed-Forward Compensation - VBAT

The ISL9500 incorporates Battery Voltage Feed-Forward Compensation, as shown in Figure 8. This compensation provides a constant Pulse Width Modulator Gain independent of battery voltage. An understanding of this gain is required for proper loop compensation. The battery voltage is connected directly to the ISL9500 by way of the VBAT pin, and the gain of the system ramp modulator is a constant 6.0.

Fault Protection

The ISL9500 protects the CPU from damaging stress levels. The overcurrent trip point is integral in preventing output shorts of varying degrees from causing current spikes that would damage a CPU. The output overvoltage and undervoltage detection features insure a safe window of operation for the CPU.

Output Voltage Monitoring

VSEN is connected to the local CORE output voltage and is used for PGOOD, undervoltage and overvoltage sensing only. Refer to the “Block Diagram”.

The voltage on VSEN is compared with two voltage levels which indicate an overvoltage or undervoltage condition of the output. Violating either of these conditions results in the PGOOD pin toggling low to indicate a problem with the output voltage.

PGOOD

As previously described, the ISL9500 PGOOD pin operates as both an input and an output. During start-up, the PGOOD pin operates as an input. Refer to Figure 10.

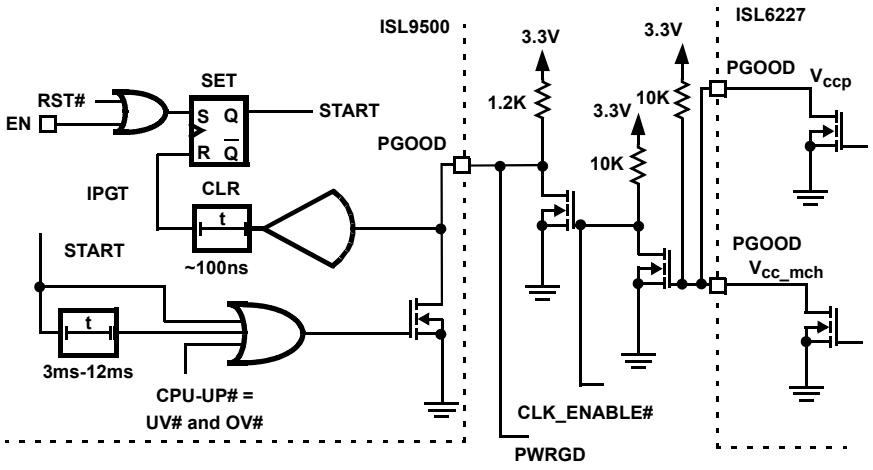


FIGURE 10. INTERNAL PGOOD CIRCUITRY FOR THE ISL9500 CORE VOLTAGE REGULATOR

Once the ISL9500 CORE regulator regulates to the “Boot” voltage, it waits for the PGOOD logic HIGH signals from the Vccp and Vcc_mch regulators. The Intersil ISL6227 is a perfect choice for these two supplies, as it is a dual regulator and has independent PGOOD functions for each supply. Once these two supplies are within regulation, $PGOOD_{Vccp}$ and $PGOOD_{Vcc\_mch}$ will be high impedance, and will allow the PGOOD of the ISL9500 to sink approximately 2.6mA to ground through the internal MOSFET, shown in Figure 10. The ISL9500 detects this current and starts an internal PGOOD timer.

The current sourced into the PGOOD pin is critical for proper start-up operation. The pullup resistor, R_{pullup} is sized to give approximately 2.6mA of current sourced into the PGOOD pin when the system is enabled and the Vccp and Vcc_mch supplies are in regulation.

As given in the electrical specifications of this document, the PGOOD MOSFET $r_{DS(on)}$ is given as 82Ω maximum. If 3.3V is used as the supply, then the pullup resistor is given by the following equation:

$$R_{Pullup} = \frac{Vsource}{2.6mA} - r_{DSON}(max) = \frac{3.3 - 0.05(3.3)}{2.6mA} - 82 \approx 1.2k\Omega \qquad \text{(EQ. 4)}$$

where Vsource is the supply minus 5% for tolerance. This will insure that approximately 2.6mA will be sourced into the PGOOD pin for worst case conditions of low supply and largest MOSFET $r_{DS(ON)}$.

Once the proper level of PGOOD current is detected, the ISL9500 then captures the VID and regulates to this value. The PGOOD timer is a function of the internal clock and switching frequency. The internal PGOOD delay can be calculated as follows:

$$\text{Timer Delay} = 3072/FSW \qquad \text{(EQ. 5)}$$

The ISL9500 controller regulates the CORE output voltage to the VID command, and once the timer has expired, the PGOOD output is allowed to go high.

NOTE: The PGOOD functions of the V_{CC_CORE}, Vccp and Vcc_mch regulators are wire OR’d together to create the system signal “PWRGD”. If any of the supplies fall outside the regulation window, their respective PGOOD pins are pulled low, which forces PWRGD low. PGOOD of the ISL9500 is internally disabled during all VID and Mode transitions.

Overvoltage

The VSEN voltage is compared with an internal overvoltage protection (OVP) reference, set to 112% of the VID voltage. If the VSEN voltage exceeds the OVP reference, a comparator simultaneously sets the OV latch, and pulls the PWM signal low. The drivers turn on the lower MOSFETs, shunting the converter output to ground. Once the output voltage falls below 102% of the set point, the high side and low side MOSFETs are held off. This prevents dumping of the output capacitors back through the output inductors and lower MOSFETs, which would cause a negative voltage on the CORE output.

This architecture eliminates the need of a high current, Schottky diode on the output. If the overvoltage condition persists, the outputs are cycled between output low and output “off”, similar to a hysteretic regulator. The OV latch is reset by cycling the VDD supply voltage to initiate a POR. Depending on the mode of operation, the overvoltage set point is 112% of the VID, Deep or Deeper Sleep set point.

Undervoltage

The VSEN pin is also compared to an undervoltage (UV) reference which is set to 84% of the VID, Deep or Deeper Sleep set point, depending on the mode of operation. If the VSEN voltage is below the UV reference for more than 32 consecutive phase clock cycles, the power good monitor triggers the PGOOD pin to go low, and latches the chip off until power is reset to the chip, or the EN pin is toggled.

Overcurrent

The RISEN resistor scales the voltage sampled across the lower MOSFET and provides current feedback proportional to the output current of each active channel. Refer to Figure 9. The ISEN currents from all the active channels are averaged together to form a scaled version of the total output current, $I_{AVERAGE}$. $I_{AVERAGE}$ is compared with an internally generated overcurrent trip threshold, which is proportional to the current sourced from the OCSET pin, I_{OCSET}. The overcurrent trip current source is programmable and described in the “Overcurrent Setting - OCSET” section of this document.

If $I_{AVERAGE}$ exceeds the I_{OCSET} level, an up/down counter is enabled. If $I_{AVERAGE}$ does not fall below I_{OCSET} within 32 phase cycle counts, the PGOOD pin transitions low and latches the chip off. If normal operation resumes within the 32 phase cycle count window, the controller will continue to operate normally. Refer to the “Block Diagram”.

NOTE: Due to “DROOP” there is inherent current limit, since load current cannot exceed the amount that would command an output voltage lower than 84% of the VID voltage. This would result in an undervoltage shutdown, and would also cause the PGOOD pin to transition low and latch the chip off.

Control Loops

The “Block Diagram” and Figure 9 show a simplified diagram of the voltage regulation and current control loops for a two-phase converter. Both voltage and current feedback are used to precisely regulate voltage and tightly control output currents, I_{L1} and I_{L2}, of the two power channels. The voltage loop is comprised of the Error Amplifier, Comparators, Internal Gate Drivers, and MOSFETs. The Error Amplifier drives the modulator to force the FB pin to the reference minus “Droop”.

Voltage Loop

The output CORE voltage feedback is applied to the Error Amplifier through the compensation network. The signal seen on the FB pin will drive the Error Amplifier output either high or low, depending on the CORE voltage. A CORE voltage level that is lower than the, as output from the 6 bit DAC, makes the amplifier output move towards a higher output voltage level. The amplifier output voltage is applied to the positive inputs of the comparators by the BALANCE summing networks. Out-of-phase sawtooth signals are applied to the two comparator inverting inputs. Increasing Error Amplifier voltage results in increased comparator output duty cycle. This increased duty cycle signal is passed through the PWM circuit to the internal gate-drive circuitry. The output of the internal gate-drive is directly connected to the gate of the MOSFETs. Increased duty cycle or ON-time for the high side MOSFET transistors results in increased output voltage, VCORE, to compensate for the low output voltage sensed.

Current Loop

The current control loop keeps the channel currents in balance. During the PWM off-time of each channel, the voltage $Vr_{DS(ON)}$, developed across the lower MOSFET is sampled. Internally, the ISEN pin is held at virtual ground during this interval, and $Vr_{DS(ON)}$ is impressed across the R_{ISEN} resistor. This provides current feedback proportional to the output current of each channel. The scaled output currents from all active channels are combined to create an average current reference $I_{AVERAGE}$, proportional to the converter total output current. This signal is then subtracted from the individual channel scaled output currents to produce a current correction signal for each channel. The current correction signal keeps each channel output current contribution balanced relative to the other active channels. Each current correction signal is subtracted from the error amplifier output and fed to the individual channel PWM circuits. For example, assume the voltage sampled across Q4 in Figure 9 is higher than that sampled across Q2. The ISEN2 current would be higher than ISEN1. When the two reference currents are averaged, they accurately represent the total output current of the converter. The reference current $I_{AVERAGE}$ is then subtracted from the ISEN currents. This results in a positive offset for Channel 2 and a negative offset for Channel 1. These offsets are subtracted from the error amplifier signal and perform phase balance correction. The V_{ERROR2} signal is reduced, while V_{ERROR1} would be increased. The PWM circuit would then reduce the pulse width to lower the output current contribution by Channel 2, while doing the opposite to Channel 1, thereby balancing channel currents.

Droop Compensation

Microprocessors and other peripherals tend to change their load current demands from near no-load to full load often during operation. These same devices require minimal output voltage deviation during a load step.

A high di/dt load step will cause an output voltage spike. The amplitude of the spike is dictated by the output capacitor ESR, multiplied by the load step magnitude, plus the output capacitor ESL, times the load step di/dt. A positive load step produces a negative output voltage spike and vice versa. A large number of low-series-impedance capacitors are often used to prevent the output voltage deviation from exceeding the tolerance of some devices. One widely accepted solution to this problem is output voltage “Droop”, or active voltage positioning.

As shown in Figure 3 and Figure 9, the average channel current is used to control the “Droop” current source, I_{DROOP}. The “Droop” current source is a controlled current source and is proportional to output current. This current source is approximately 87% of the averaged ISEN currents. The Droop current is sourced out of the SOFT pin through the Droop resistor and returns through the EA+ pin. This creates a “Droop” voltage V_{DROOP}, which subtracts from the reference voltage on SOFT to generate the voltage set point for the CORE regulator.

Knowing that the Droop Current, sourced out of the SOFT pin, a “Droop” resistor R_{DROOP}, can be selected to provide the amount of voltage “Droop” required at full load. The selection of this resistor is explained in the following section.

Selection of RDROOP

LOAD LINE EXAMPLE shows a static “Droop” load line for the 1.484V Active Mode. The ISL9500, as previously mentioned, allows the programming of the load line slope by the selection of the RDROOP resistor.

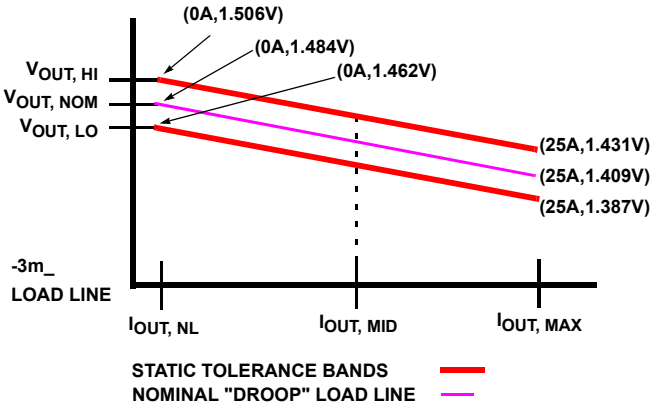


FIGURE 11. LOAD LINE EXAMPLE

For example, Droop = 0.003 (Ω). Therefore, 25A of full load current equates to a 0.075V Droop output voltage from the VID setpoint. Refer to Figure 3 and Figure 9, R_{DROOP} can be selected based on R_{ISEN} which is calculated through Equation 3, $R_{(DSON)}$, and Droop as per the Block Diagram or the following equation:

$$R_{DROOP} = 2.3 \cdot (\text{Droop}) \cdot \frac{R_{ISEN}}{\frac{r_{(DSON)}}{M}} (\Omega) \qquad \text{(EQ. 6)}$$

Diode Emulation

Diode emulation allows for higher converter efficiency under light-load situations. With diode emulation active, the ISL9500 will detect the zero current crossing of the output inductor and turn off LGATE. This ensures that discontinuous conduction mode (DCM) is achieved. In DCM, conduction losses are reduced in the Low-Side MOSFET, consequently boosting efficiency. The ISL9500 operates in DCM in both Deep and Deeper Sleep mode.

Component Selection Guidelines

OUTPUT CAPACITOR SELECTION

Output capacitors are required to filter the output inductor current ripple and supply the transient load current. The filtering requirements are a function of the channel switching frequency and the output ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current.

The microprocessor will produce transient load rates as high as 30A/ns. High frequency, ceramic capacitors are used to supply the initial transient current and slow the rate-of-change seen by the bulk capacitors. Bulk filter capacitor values are generally determined by the ESR (Effective Series Resistance) and voltage rating requirements rather than actual capacitance requirements. To meet the stringent transient response requirements (15) 2.2µF, 0612 “Flip Chip” high frequency, ceramic capacitors are placed very close the Processor power pins, with care being taken not to add inductance in the circuit board traces that could cancel the usefulness of these low inductance components.

Specialized low-ESR capacitors, intended for switching regulator applications, are recommended for the bulk capacitors. The bulk capacitor ESR and ESL determine the output ripple voltage and the initial voltage drop following a high slew-rate transient edge. Recommended are at least (4) 4V, 220µF Sanyo Sp-Cap capacitors in parallel, or (5) 330µF SP-Cap style capacitors. These components should be laid out very close to the load.

As the sense trace for VSEN may be long and routed close to switching nodes, a 1.0µF ceramic decoupling capacitor is located between VSEN and ground at the ISL9500.

Output Inductor Selection

The output inductor is selected to meet the voltage ripple requirements and minimize the converter response time to a load transient. In a multi-phase converter topology, the ripple current of one active channel partially cancels with the other active channels to reduce the overall ripple current. The reduction in total output ripple current results in a lower overall output voltage ripple.

The inductor selected for the power channels determines the channel ripple current. Increasing the value of inductance reduces the total output ripple current and total output voltage ripple; however, increasing the inductance value will slow the converter response time to a load transient.

One of the parameters limiting the converter response time to a load transient is the time required to slew the inductor current from its initial current level to the transient current level. During this interval, the difference between the two levels must be supplied by the output capacitance.

Minimizing the response time can minimize the output capacitance required.

The channel ripple can be reasonably approximated by the following equation:

$$\Delta I_{CH} = \frac{V_{IN} - V_{OUT}}{F_{SW} \bullet L} \bullet \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 7)}$$

The total output ripple current can be approximated from the curves in Figure 12.

They provide the total ripple current as a function of duty cycle and number of active channels, normalized to the parameter K_{NORM} at zero duty cycle,

$$K_{NORM} = \frac{V_{OUT}}{L \bullet F_{SW}} \quad \text{(EQ. 8)}$$

Where L is the channel inductor value.

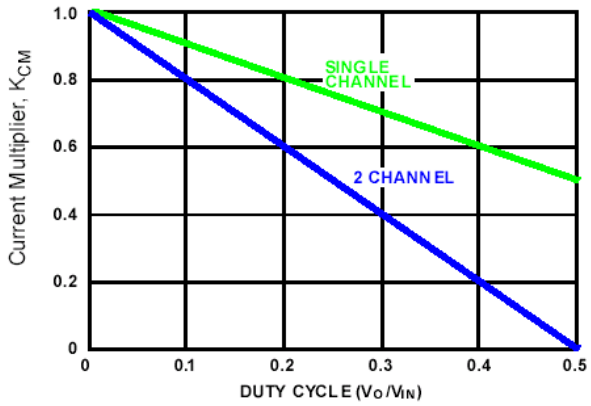


FIGURE 12. OUTPUT RIPPLE CURRENT MULTIPLIER vs DUTY CYCLE

Find the intersection of the active channel curve and duty cycle for your particular application. The resulting ripple current multiplier from the y-axis is then multiplied by the normalization factor K_{NORM}, to determine the total output ripple current for the given application. Find the intersection of the active channel curve and duty cycle for your particular application. The resulting ripple current multiplier from the y-axis is then multiplied by the normalization factor K_{NORM}, to determine the total output ripple current for the given application.

$$\Delta I_{TOTAL} = K_{NORM} \bullet K_{CM} \quad \text{(EQ. 9)}$$

INPUT CAPACITOR SELECTION

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use ceramic capacitors for the high frequency decoupling, and bulk capacitors to supply the RMS current. Small ceramic capacitors must be placed very close to the upper MOSFET to suppress the voltage induced in the parasitic circuit impedances.

Two important parameters to consider when selecting the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select a bulk capacitor with voltage, and current ratings above the maximum input voltage and the largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current requirement for a converter design can be approximated with the aid of Figure 13.

Follow the curve for the number of active channels in the converter design. Next determine the worst case duty cycle for the converter and find the intersection of this value and the active channel curve. The worst case duty cycle is defined as the maximum operating CORE output voltage divided by the minimum operating battery voltage. Find the corresponding y-axis value, which is the current multiplier. Multiply the total full load output current, not the channel value, by the current multiplier value found, and the result is the RMS input current which must be supported by the input capacitors.

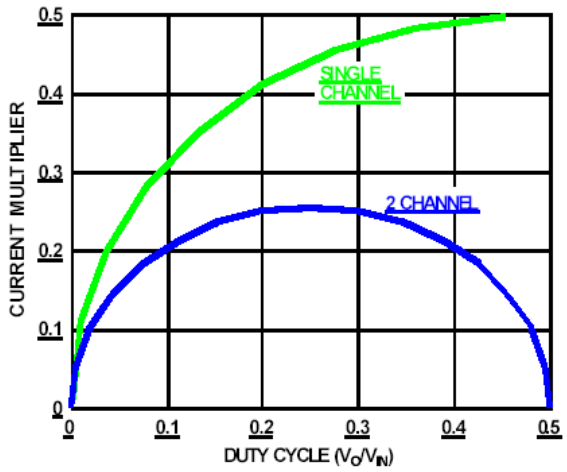


FIGURE 13. INPUT RMS RIPPLE CURRENT MULTIPLIER

MOSFET Selection and Considerations

For 25A of load current, it is suggested that 2 channel operation with (3) MOSFETs per channel be implemented. This configuration would be: (1) High Switching Frequency, Low Gate Charge MOSFET for the Upper, and (2) Low $r_{DS(ON)}$ MOSFETs for the Lowers.

In high-current PWM applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components: conduction loss and switching loss. These losses are distributed between the upper and lower MOSFETs according to duty cycle of the converter. Refer to the P_{UPPER} and P_{LOWER} equations below. The conduction losses are the main component of power dissipation for the lower MOSFETs. Only the upper MOSFETs have significant switching losses, since the lower devices turn on and off into near zero voltage. The following equations assume linear

voltage-current transitions and do not model power loss due to the reverse-recovery of the lower MOSFETs body diode. The gate-charge losses are dissipated in the ISL9500 drivers and do not heat the MOSFETs; however, large gate-charge increases the switching time t_{SW}, which increases the upper MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature, at high ambient temperature, by calculating the temperature rise according to package thermal-resistance specifications.

$$P_{LOWER} = \frac{I_O^2 \times r_{DS(ON)} \times (V_{IN} - V_{OUT})}{V_{IN}} \quad \text{(EQ. 10)}$$

$$P_{UPPER} = \frac{I_O^2 \times r_{DS(ON)} \times V_{OUT}}{V_{IN}} + \frac{I_O \times V_{IN} \times t_{SW} \times F_{SW}}{2} \quad \text{(EQ. 11)}$$

Typical Application - 2 Phase Converter Using ISL9500 PWM Controller - 38 Lead TSSOP

Figure 14 shows the ISL9500, Synchronous Buck Converter circuit used to provide the CORE voltage regulation. The circuit uses 2 channels for delivering up to 25A steady state current, and has a 250kHz channel switching frequency. This circuit also switches to single channel operation for Deep and Deeper Sleep modes of operation. For thermal compensation, PTC resistors are used as sense resistors. The output capacitance is less than 3mΩ of ESR, and are (4) 220µF, 4V Sp-Cap parts in parallel with (35) high frequency, 10µF ceramic capacitors.

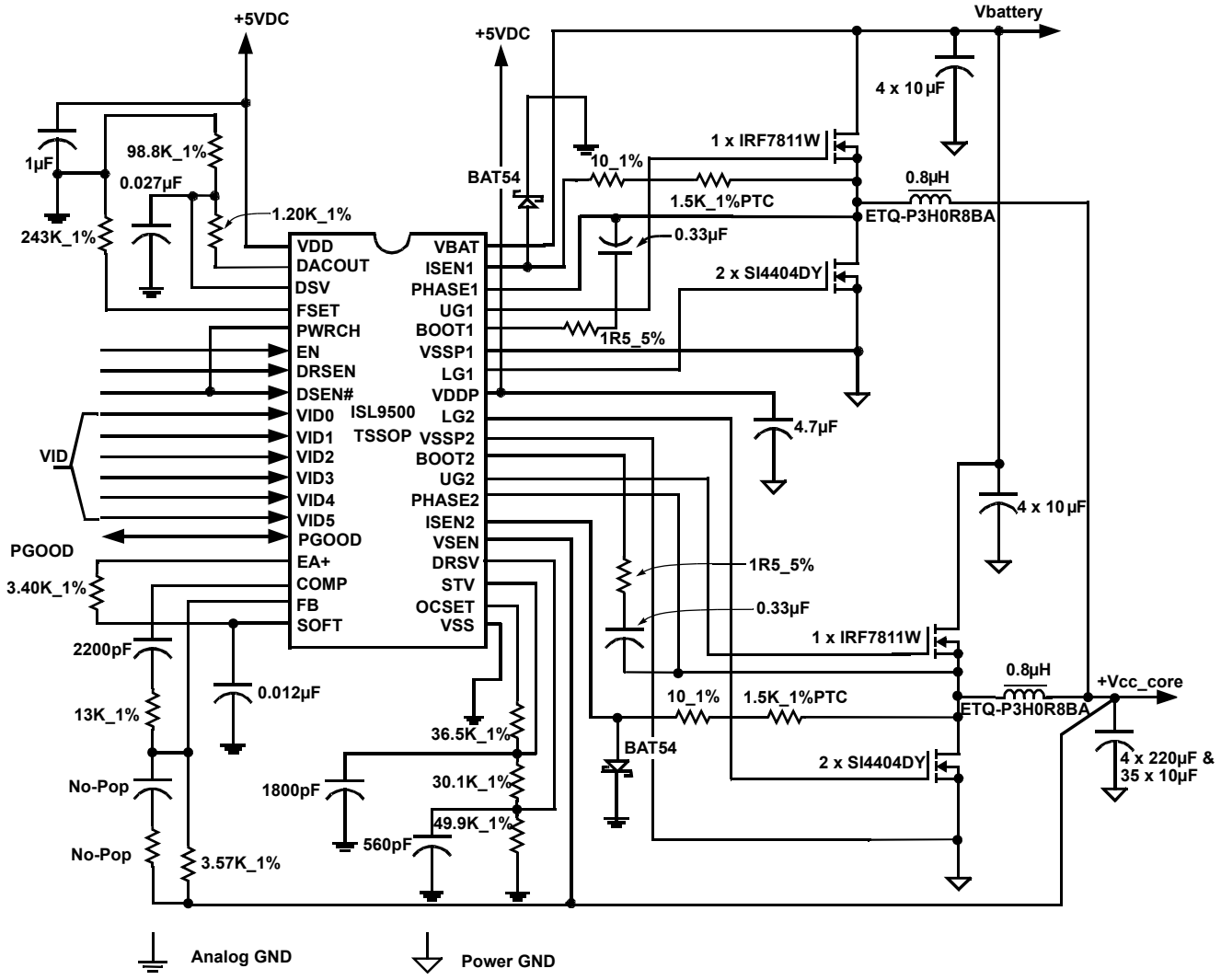
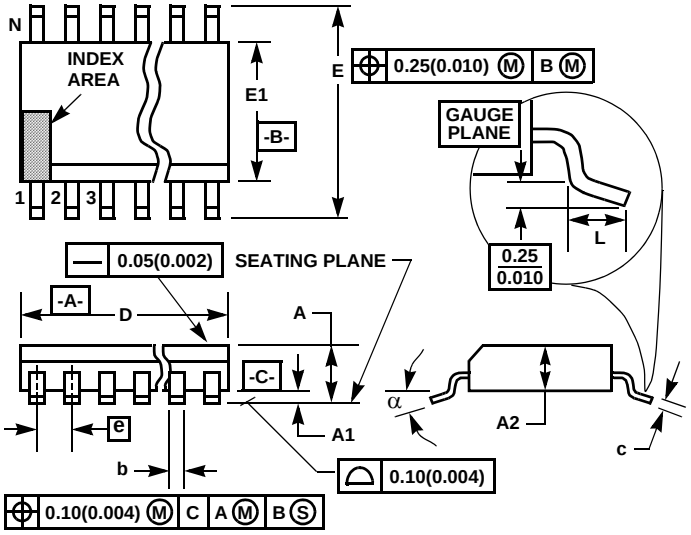


FIGURE 14. TYPICAL APPLICATION CIRCUIT FOR CORE VOLTAGE REGULATOR

Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-BD-1, Issue F.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

M38.173

38 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-153-BD-1 ISSUE F)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.051	0.80	1.05	-
b	0.0075	0.0106	0.17	0.27	9
c	0.0035	0.0079	0.09	0.20	-
D	0.378	0.386	9.60	9.80	3
E1	0.169	0.177	4.30	4.50	4
e	0.0197 BSC		0.500 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	38		38		7
α	0^o	8^o	0^o	8^o	-

Rev. 0 1/03