Never stop thinking

# TLE8386-2EL

Basic Smart Boost Controller

## Data Sheet

Rev. 1.0, 2010-10-25

Automotive Power

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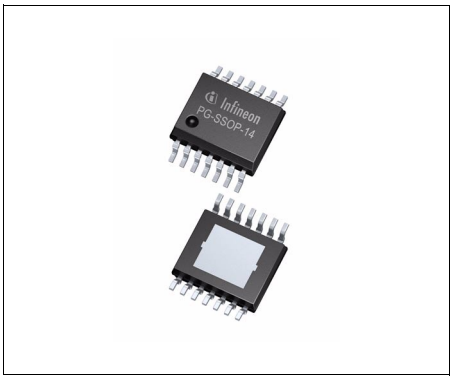
# 1 Overview




**PG-SSOP-14**

### Features

- Wide Input Voltage Range from 4.75 V to 45 V
- Constant Current or Constant Voltage Regulation
- Very Low Shutdown Current: IQ< 2µA
- Flexible Switching Frequency Range, 100 kHz to 700 kHz
- Synchronization with external clock source
- Available in a small thermally enhanced PG-SSOP-14 package
- Internal 5 V Low Drop Out Voltage Regulator
- Output Overvoltage Protection
- External Soft Start adjustable by capacitor
- Over Temperature Shutdown
- Automotive AEC Qualified
- Green Product (RoHS) Compliant

### Description

The TLE8386-2EL is a boost controller with built in protection features. The main function of this device is to step-up (boost) an input voltage to a larger output voltage. The switching frequency is adjustable from 100 kHz to 700 kHz and can be synchronized to an external clock source. The TLE8386-2EL features an enable function reducing the shut-down current consumption to < 2 µA. The current mode regulation scheme of this device provides a stable regulation loop maintained by small external compensation components. The integrated soft-start feature with external components for adjustment limits the current peak as well as voltage overshoot at start-up. This IC is suited for use in the harsh automotive environments and provides protection functions such as output overvoltage protection and over temperature shutdown.

| Type | Package | Marking |
|---|---|---|
| TLE8386-2EL | PG-SSOP-14 | TLE8386-2EL |

## 2 Block Diagram

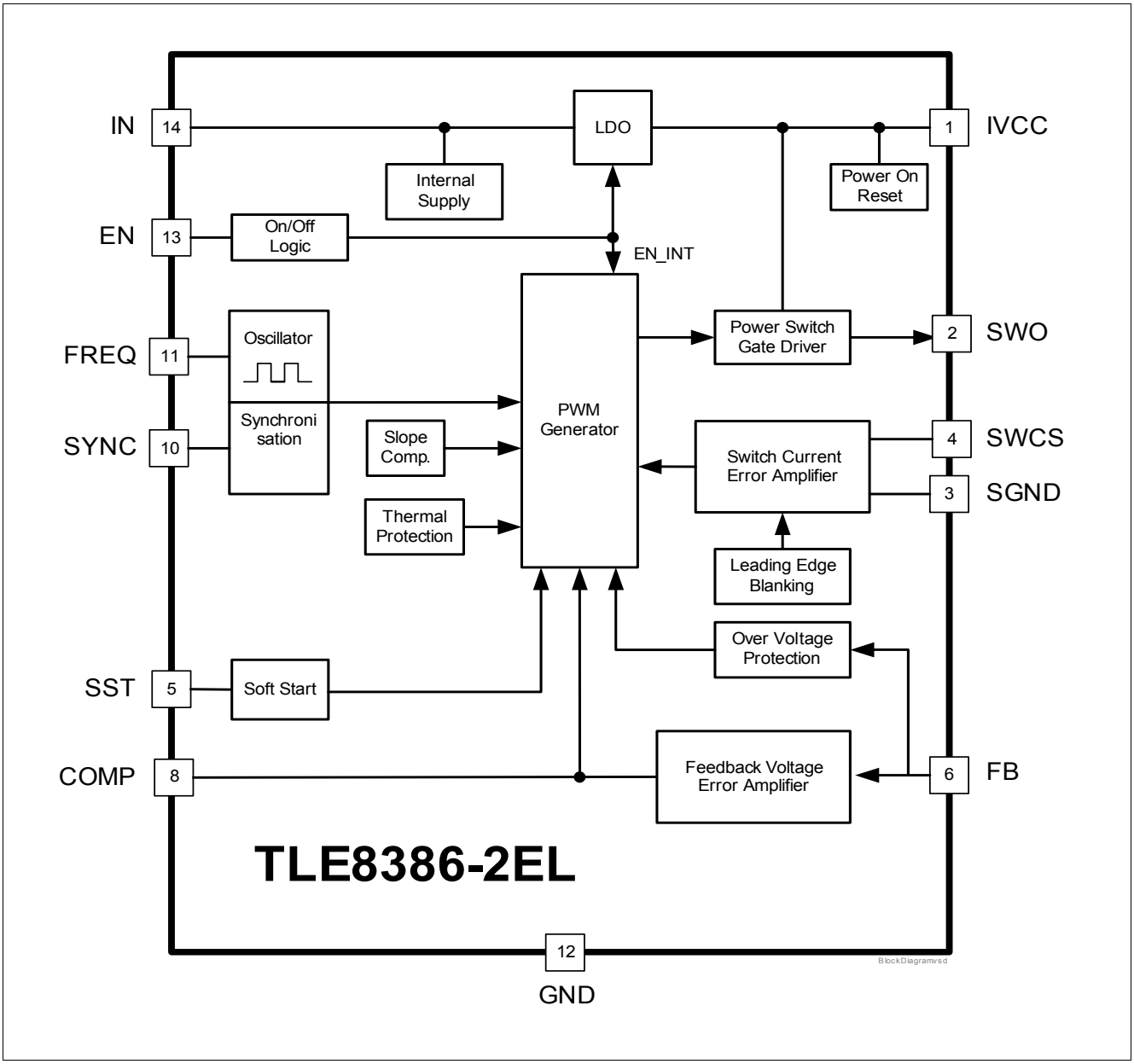



**Figure 1 Block Diagram**

# 3 Pin Configuration

## 3.1 Pin Assignment

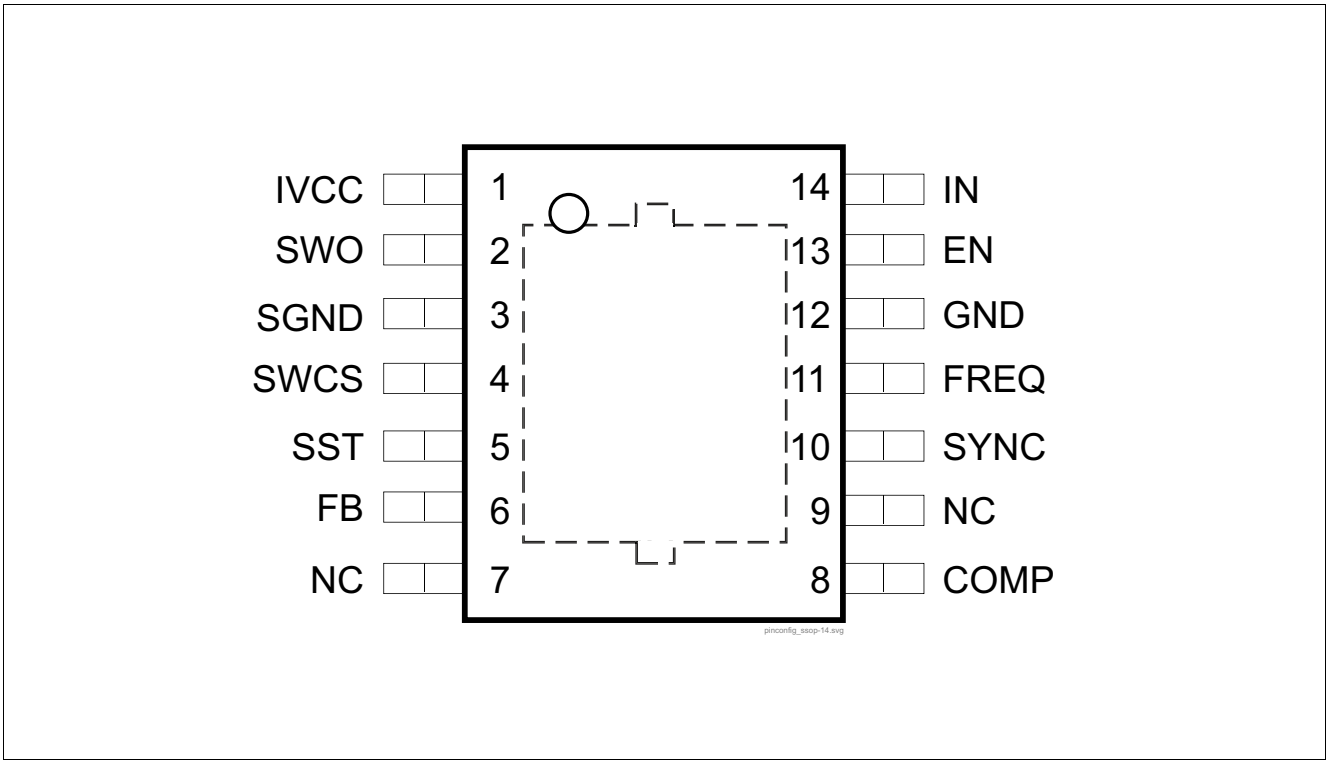



**Figure 2 Pin Configuration**

## 3.2 Pin Definitions and Functions

| Pin | Symbol | Function |
|---|---|---|
| 1 | IVCC | **Internal LDO Output;**<br>Used for internal biasing and gate drive. Do not leave open, bypass with external capacitor. Do not connect other circuitry to this pin. |
| 2 | SWO | **Switch Output;**<br>Connect to the gate of external boost converter switching MOSFET. |
| 3 | SGND | **Current Sense Ground;**<br>Ground return for current sense switch, connect to bottom side of sense resistor. |
| 4 | SWCS | **Current Sense Input;**<br>Detects the peak current through switch, connect to high side of sense resistor. |
| 5 | SST | **Soft Start;**<br>Connect an external capacitor to adjust the soft start ramp, do not leave open. |
| 6 | FB | **Feedback;**<br>Output voltage feedback, connect to output voltage via resistor divider from output capacitor to ground. |
| 7 | NC | **Not Connected;** |
| 8 | COMP | **Compensation Input;**<br>Connect R and C network to improve the stability of the regulation loop. |

| Pin | Symbol | Function |
|---|---|---|
| 9 | NC | **Not Connected;** |
| 10 | SYNC | **Sync;**<br>Synchronization Input, if feature synchronization is not used, leave open. |
| 11 | FREQ | **Frequency Select Input;**<br>Connect external resistor to GND to set frequency, do not leave open. |
| 12 | GND | **Ground;**<br>Connect to system ground. |
| 13 | EN | **Enable;**<br>Apply logic high signal to enable device. |
| 14 | IN | **Supply Input;**<br>Supply for internal biasing, connect to input voltage. |
| Exposed Pad | | Connect to GND. |

# 4 General Product Characteristics

## 4.1 Absolute Maximum Ratings

**Absolute Maximum Ratings[1)]**

$T_j$ = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | | Min. | Max. | | |
| **Voltages** | | | | | | |
| 4.1.1 | IN<br>Supply Input | $V_{IN}$ | -0.3 | 45 | V | |
| 4.1.2 | EN<br>Enable Input | $V_{EN}$ | -40 | 45 | V | |
| 4.1.3 | FB;<br>Feedback Error Amplifier Input | $V_{FB}$ | -0.3 | 5.5 | V | |
| 4.1.4 | | | -0.3 | 6.2 | V | $t$ < 10s |
| 4.1.5 | SWCS<br>Switch Current Sense Input | $V_{SWCS}$ | -0.3 | 5.5 | V | |
| 4.1.6 | | | -0.3 | 6.2 | V | $t$ < 10s |
| 4.1.7 | SWO<br>Switch Gate Drive Output | $V_{SWO}$ | -0.3 | 5.5 | V | |
| 4.1.8 | | | -0.3 | 6.2 | V | $t$ < 10s |
| 4.1.9 | SGND<br>Current Sense Switch GND | $V_{SGND}$ | -0.3 | 0.3 | V | |
| 4.1.10 | COMP<br>Compensation Input | $V_{COMP}$ | -0.3 | 5.5 | V | |
| 4.1.11 | | | -0.3 | 6.2 | V | $t$ < 10s |
| 4.1.12 | FREQ; Frequency Input | $V_{FREQ}$ | -0.3 | 5.5 | V | |
| 4.1.13 | | | -0.3 | 6.2 | V | $t$ < 10s |
| 4.1.14 | SYNC; Synchronization Input | $V_{SYNC}$ | -0.3 | 5.5 | V | |
| 4.1.15 | | | -0.3 | 6.2 | V | $t$ < 10s |
| 4.1.16 | SST; Softstart Setting Input | $V_{SST}$ | -0.3 | 5.5 | V | |
| 4.1.17 | | | -0.3 | 6.2 | V | $t$ < 10s |
| 4.1.18 | IVCC<br>Internal Linear Voltage Regulator Output | $V_{IVCC}$ | -0.3 | 5.5 | V | |
| 4.1.19 | | | -0.3 | 6.2 | V | $t$ < 10s |
| **Temperatures** | | | | | | |
| 4.1.20 | Junction Temperature | $T_j$ | -40 | 150 | °C | – |
| 4.1.21 | Storage Temperature | $T_{stg}$ | -55 | 150 | °C | – |

**Absolute Maximum Ratings**[1)]

$T_j$ = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | | Min. | Max. | | |
| **ESD Susceptibility** | | | | | | |
| 4.1.22 | ESD Resistivity to GND | $V_{ESD,HBM}$ | -2 | 2 | kV | HBM[2)] |
| 4.1.23 | ESD Resistivity to GND | $V_{ESD,CDM}$ | -500 | 500 | V | CDM[3)] |
| 4.1.24 | ESD Resistivity Pin 1, 7, 8, 14 (corner pins) to GND | $V_{ESD,CDM,C}$ | -750 | 750 | V | CDM[3)] |

1) Not subject to production test, specified by design.

2) ESD susceptibility, Human Body Model “HBM” according to EIA/JESD 22-A114B

3) ESD susceptibility, Charged Device Model “CDM” EIA/JESD22-C101 or ESDA STM5.3.1

*Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

*Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

## 4.2 Functional Range

| Pos. | Parameter | Symbol | Limit Values | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | | Min. | Max. | | |
| 4.2.1 | Supply Voltage Input | $V_{IN}$ | 4.75 | 45 | V | $V_{IVCC} > V_{IVCC,RTH,d}$ |

*Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

## 4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| 4.3.1 | Junction to Case[1)] | $R_{thJC}$ | – | 10 | – | K/W | – |
| 4.3.2 | Junction to Ambient[1) 2)] | $R_{thJA}$ | – | 47 | – | K/W | 2s2p |
| 4.3.3 | | $R_{thJA}$ | – | 54 | – | K/W | 1s0p + 600 mm$^2$ |
| 4.3.4 | | $R_{thJA}$ | – | 64 | – | K/W | 1s0p + 300 mm$^2$ |

1) Not subject to production test, specified by design.

2) Specified $R_{thJA}$ value is according to JEDEC 2s2p (JESD 51-7) + (JESD 51-5) and JEDEC 1s0p (JESD 51-3) + heatsink area at natural convection on FR4 board;

# 5 Boost Regulator

## 5.1 Description

The TLE8386-2 boost (step-up) regulator provides a higher output voltage than input voltage. The PWM controller measures the output voltage via a resistor divider connected between Pin FB and ground, and determines the appropriate pulse width duty cycle (on time). An over voltage protection switches off the converter case if the voltage at Pin FB exceeds the over voltage limit. If the connection to the output voltage resistor divider should be lost, an internal current source connected to Pin FB will draw the voltage above this limit and shut the external MOSFET off. The current mode controller has a built-in slope compensation to prevent sub-harmonic oscillations which is a characteristic of current mode controllers operating at high duty cycles (>50% duty). An additional built-in feature is an integrated soft start that limits the current through the inductor and the external power switch during Initialization.

The soft start time $T_{SS}$ is adjustable using an external capacitor $C_{SST}$:

$$T_{SS} = C_{SST} \times \frac{2{,}00\,V}{10\,\mu A}$$

The switching frequency may be adjusted by using an external resistor (please refer to chapter **Oscillator and Synchronization**). If synchronization to an external frequency source is used, the internal frequency has to be adjusted close to this external source.

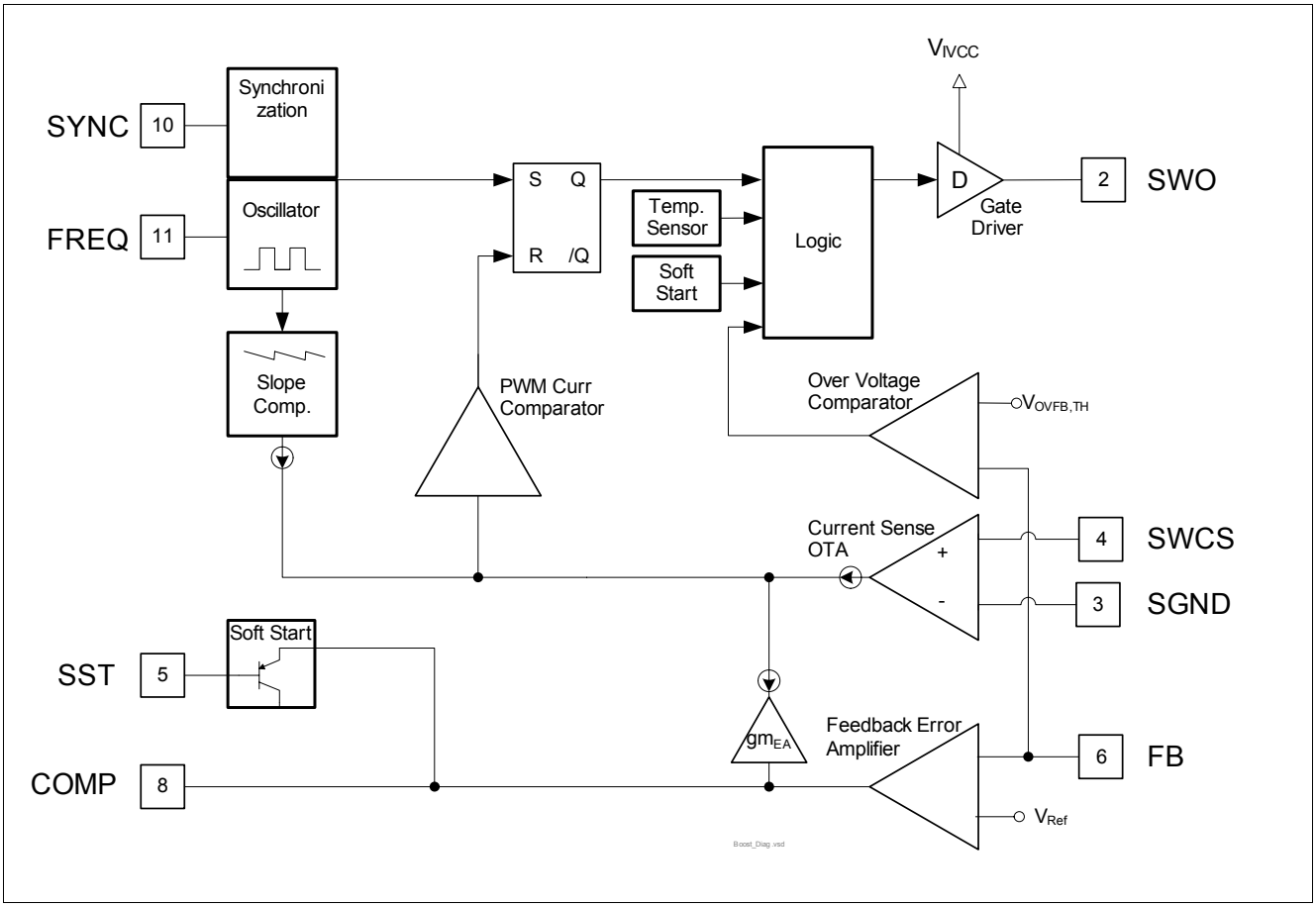



**Figure 3 Boost Regulator Block Diagram**

## 5.2 Electrical Characteristics

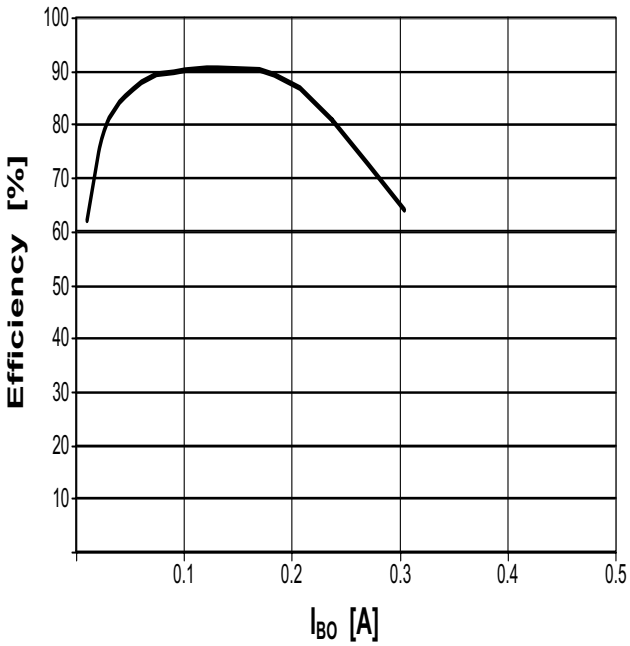
$V_{IN}$ = 6V to 40V; $T_j$ = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| *Boost Regulator:* | | | | | | | |
| 5.2.1 | Feedback Reference Voltage | $V_{FB}$ | 2.32. | 2.5 | 2.62 | V | $V_{IN}$ = 19 V; $I_{BO}$ = 100 to 500 mA |
| 5.2.2 | Voltage Line Regulation | $\Delta V_{REF}$ /$\Delta V_{IN}$ | – | – | 0.15 | %/V | $V_{IN}$ = 6 to 19 V; $V_{BO}$= 30 V; $I_{BO}$ = 100 mA **Figure 8** |
| 5.2.3 | Voltage Load Regulation | $\Delta V_{FB}$ /$\Delta I_{BO}$ | – | – | 5 | %/A | $V_{IN}$ = 13V; $V_{BO}$ = 30V; $I_{BO}$ = 100 to 500 mA **Figure 8** |
| 5.2.4 | Switch Peak Over Current Threshold | $V_{SWCS}$ | 120 | 150 | 180 | mV | $V_{IN}$ = 6 V $V_{FB}$ < $V_{FBOV}$ $V_{COMP}$ = 3.5V |
| 5.2.5 | Current to Softstart setting Capacitor | $I_{SST}$ | -8 | -10 | -16 | µA | |
| 5.2.6 | Feedback Input Current | $I_{FB}$ | | -200 | | nA | |
| 5.2.7 | Switch Current Sense Input Current | $I_{SWCS}$ | -10 | -50 | -100 | µA | $V_{SWCS}$ = 150 mV |
| 5.2.8 | Input Undervoltage Shutdown | $V_{IN,off}$ | 3.75 | – | – | V | $V_{IN}$ decreasing |
| 5.2.9 | Input Voltage Startup | $V_{IN,on}$ | – | – | 4.75 | V | $V_{IN}$ increasing |
| *Gate Driver for Boost Switch* | | | | | | | |
| 5.2.10 | Gate Driver Peak Sourcing Current[1)] | $I_{SWO,SRC}$ | – | -380 | – | mA | $V_{SWO}$ = 3.5V |
| 5.2.11 | Gate Driver Peak Sinking Current[1)] | $I_{SWO,SNK}$ | – | 550 | – | mA | $V_{SWO}$ = 1.5V |
| 5.2.12 | Gate Driver Output Rise Time | $t_{R,SWO}$ | – | 30 | 60 | ns | $C_{L,SWO}$ = 3.3nF; $V_{SWO}$ = 1V to 4V |
| 5.2.13 | Gate Driver Output Fall Time | $t_{F,SWO}$ | – | 20 | 40 | ns | $C_{L,SWO}$ = 3.3nF; $V_{SWO}$ = 1V to 4V |
| 5.2.14 | Gate Driver Output Voltage[1)] | $V_{SWO}$ | 4.5 | – | 5.5 | V | $C_{L,SWO}$ = 3.3nF; |

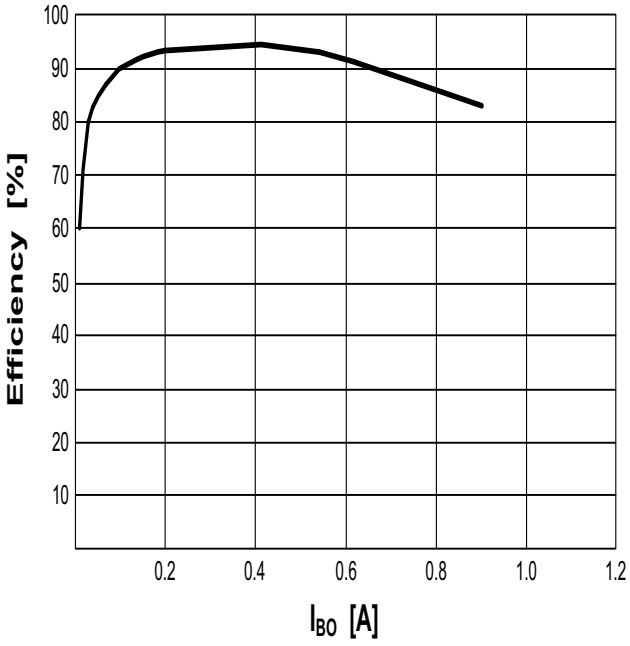
1) Not subject to production test, specified by design

**Efficiency dependingon**
**Input Voltage $V_{IN}$ and output Current $I_{BO}$**

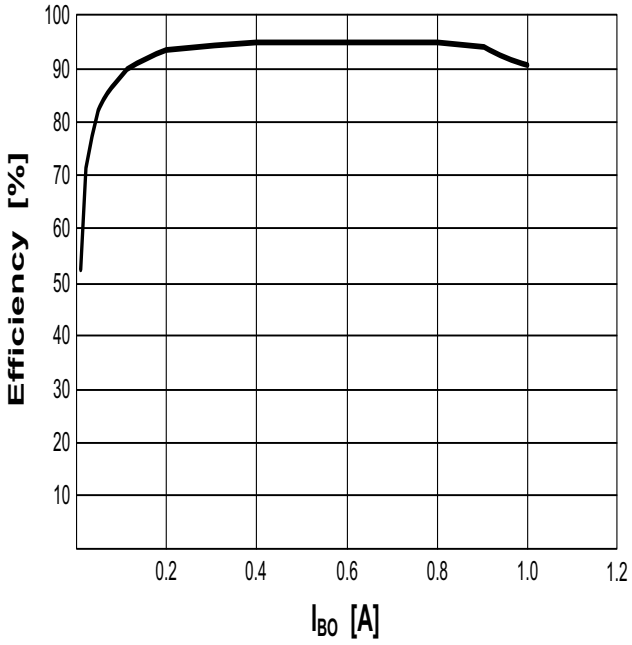
Efficiency for $V_{IN}$ = 6V



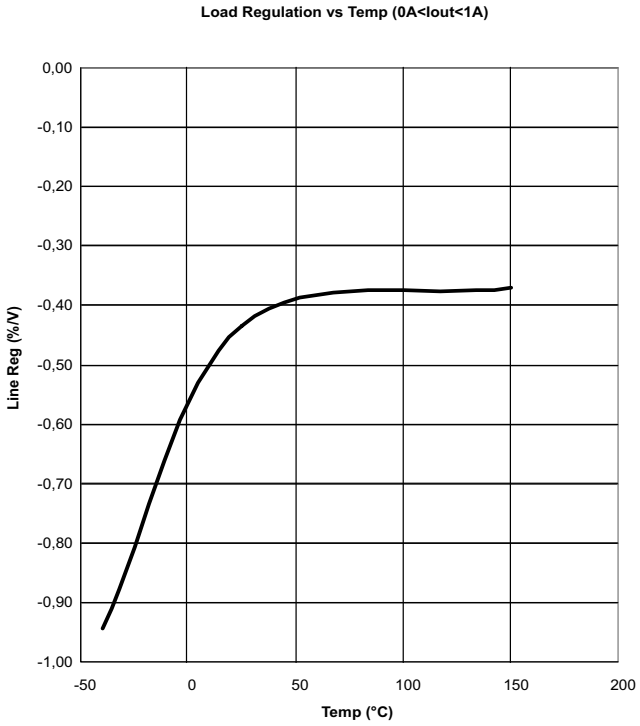

Efficiency for $V_{IN}$ = 12V



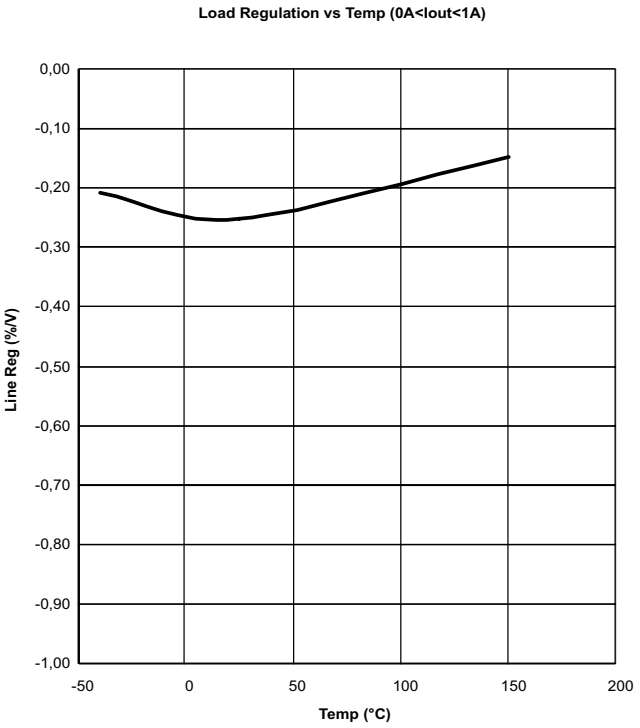

Efficiency for $V_{IN}$ = 19V



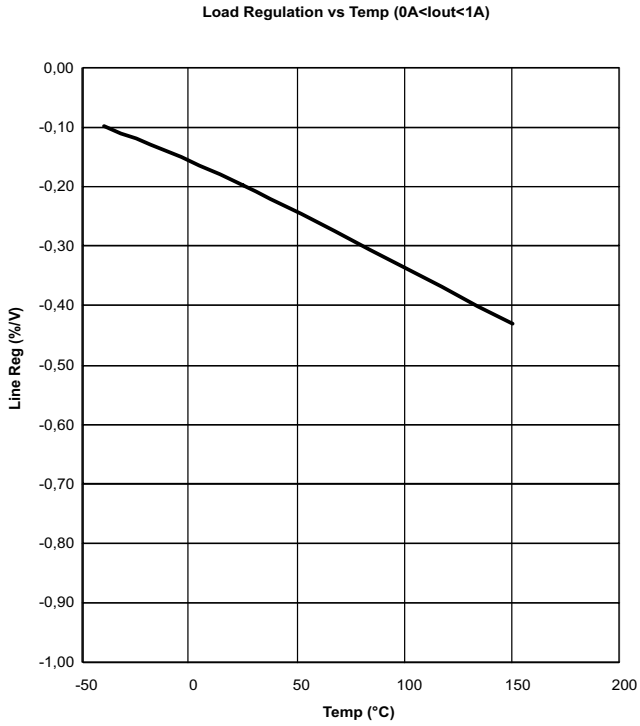
### Load regulation
### Input Voltage $V_{IN}$ = 6V




### Load regulation
### Input Voltage $V_{IN}$ = 13.5




### Load regulation
### Input Voltage $V_{IN}$ = 19V



# 6 Oscillator and Synchronization

## 6.1 Description

R_OSC vs. switching frequency

The internal oscillator is used to determine the switching frequency of the boost regulator. The switching frequency can be selected from 100 kHz to 700 kHz with an external resistor to GND. To set the switching frequency with an external resistor the following formula can be applied.

$$R_{FREQ} = \frac{1}{\left(141 \times 10^{-12}\left[\frac{s}{\Omega}\right]\right) \times \left(f_{FREQ}\left[\frac{1}{s}\right]\right)} - \left(3.5 \times 10^{3}\left[\Omega\right]\right)\ \left[\Omega\right]$$

In addition, the oscillator is capable of changing from the frequency set by the external resistor to a synchronized frequency from an external clock source. If an external clock source is provided on the pin SYNC, the internal oscillator should adjusted close to this frequency. Then it synchronizes to this external clock frequency and the boost regulator switches at the synchronized frequency. The synchronization frequency capture range is from 250 kHz to 700 kHz.

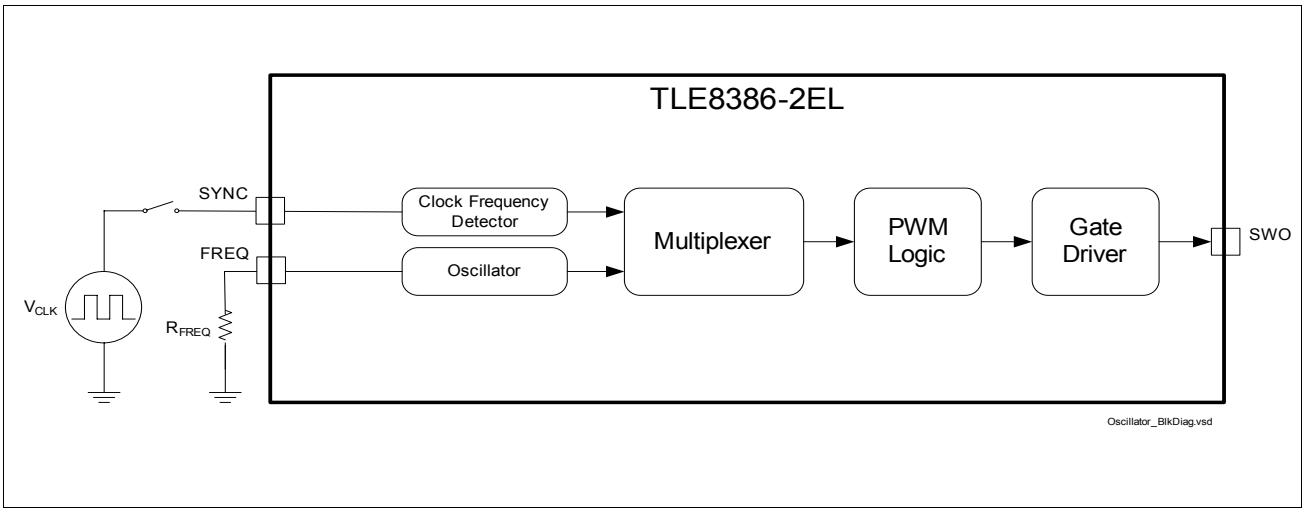



**Figure 4 Oscillator and Synchronization Block Diagram and Simplified Application Circuit**

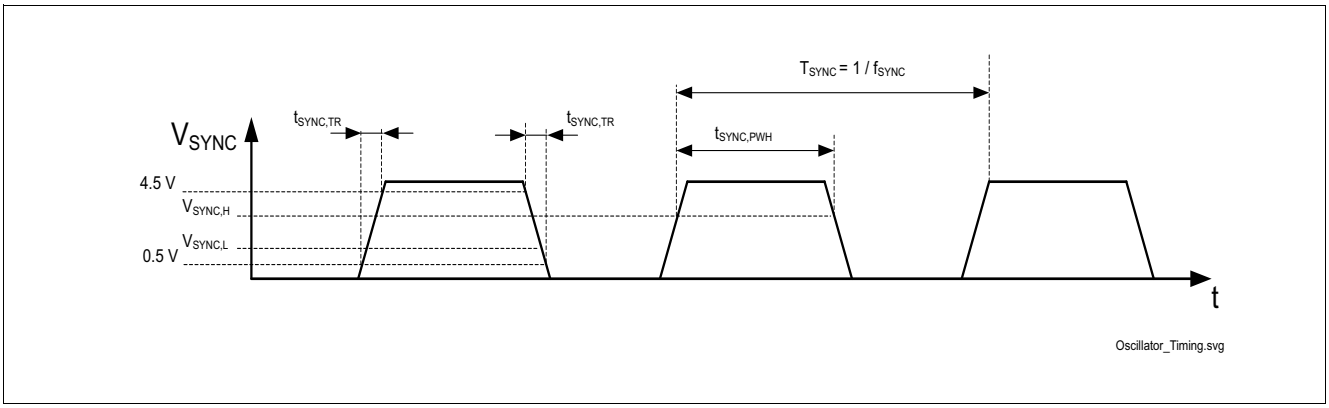



**Figure 5 Synchronization Timing Diagram**

## 6.2 Electrical Characteristics

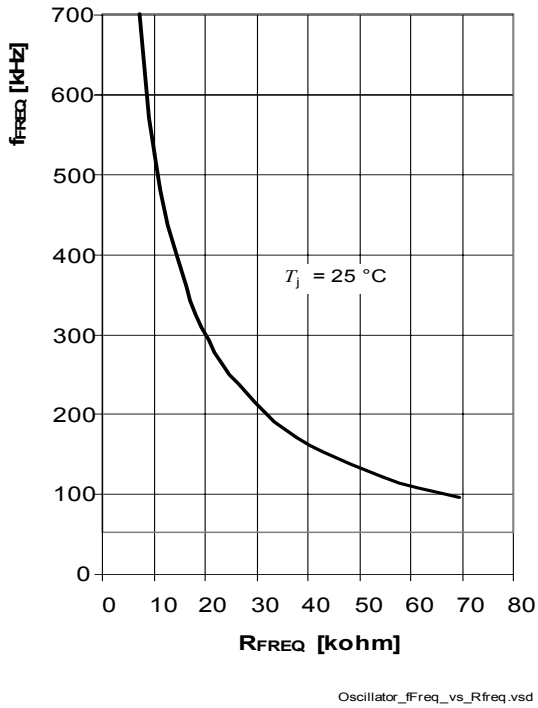
$V_{IN}$ = 6V to 40V; $T_j$ = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| *Oscillator:* | | | | | | | |
| 6.2.1 | Oscillator Frequency | $f_{FREQ}$ | 250 | 300 | 350 | kHz | $R_{FREQ}$ = 20kΩ |
| 6.2.2 | Oscillator Frequency Adjustment Range | $f_{FREQ}$ | 100 | – | 700 | kHz | 17% internal tolerance + external resistor tolerance |
| 6.2.3 | FREQ Supply Current | $I_{FREQ}$ | – | – | -700 | µA | $V_{FREQ}$ = 0 V |
| *Synchronization* | | | | | | | |
| 6.2.4 | SYNC input internal pull-down | $R_{SYNC}$ | 150 | 250 | 350 | kΩ | $V_{SYNC}$= 5V |
| 6.2.5 | Maximum Duty Cycle | $D_{MAX,fixed}$ | 90 | 93 | 95 | % | Fixed frequency mode |
| 6.2.6 | Maximum Duty Cycle | $D_{MAX,sync}$ | 88 | – | – | % | Synchronization mode, ratio between synchronization and internal frequency (set by resistor) is 0.8 to 1.2 |
| 6.2.7 | Synchronization Frequency Capture Range | $f_{SYNC}$ | 250 | – | 700 | kHz | ratio between synchronization and internal frequency (set by resistor) is 0.8 to 1.2 |
| 6.2.8 | Synchronization Signal Duty cycle | $T_{D\_SYNC}$ | 20 | | 80 | % | |
| 6.2.9 | Synchronization Signal High Logic Level Valid | $V_{SYNC,H}$ | 3.0 | – | – | V | 1) |
| 6.2.10 | Synchronization Signal Low Logic Level Valid | $V_{SYNC,L}$ | – | – | 0.8 | V | 1) |

1) Synchronization of external SWO ON signal to falling edge

## Typical Performance Characteristics of Oscillator

### Switching Frequency $f_{SW}$ versus Frequency Select Resistor to GND $R_{FREQ}$



# 7 Enable Function

## 7.1 Description

The enable function powers on or off the device. A valid logic low signal on enable pin EN powers off the device and current consumption is less than 2 µA. A valid logic high enable signal on enable pin EN powers on the device.

The Enable Startup Time $t_{EN,START}$ is the time between the Enable signal is recognized as valid and the device starts to switch. During this period of time the internal supplies, bandgap are initalized and reach their nominal values. The TLE8386-2 will start to switch after the nominal values are reached.

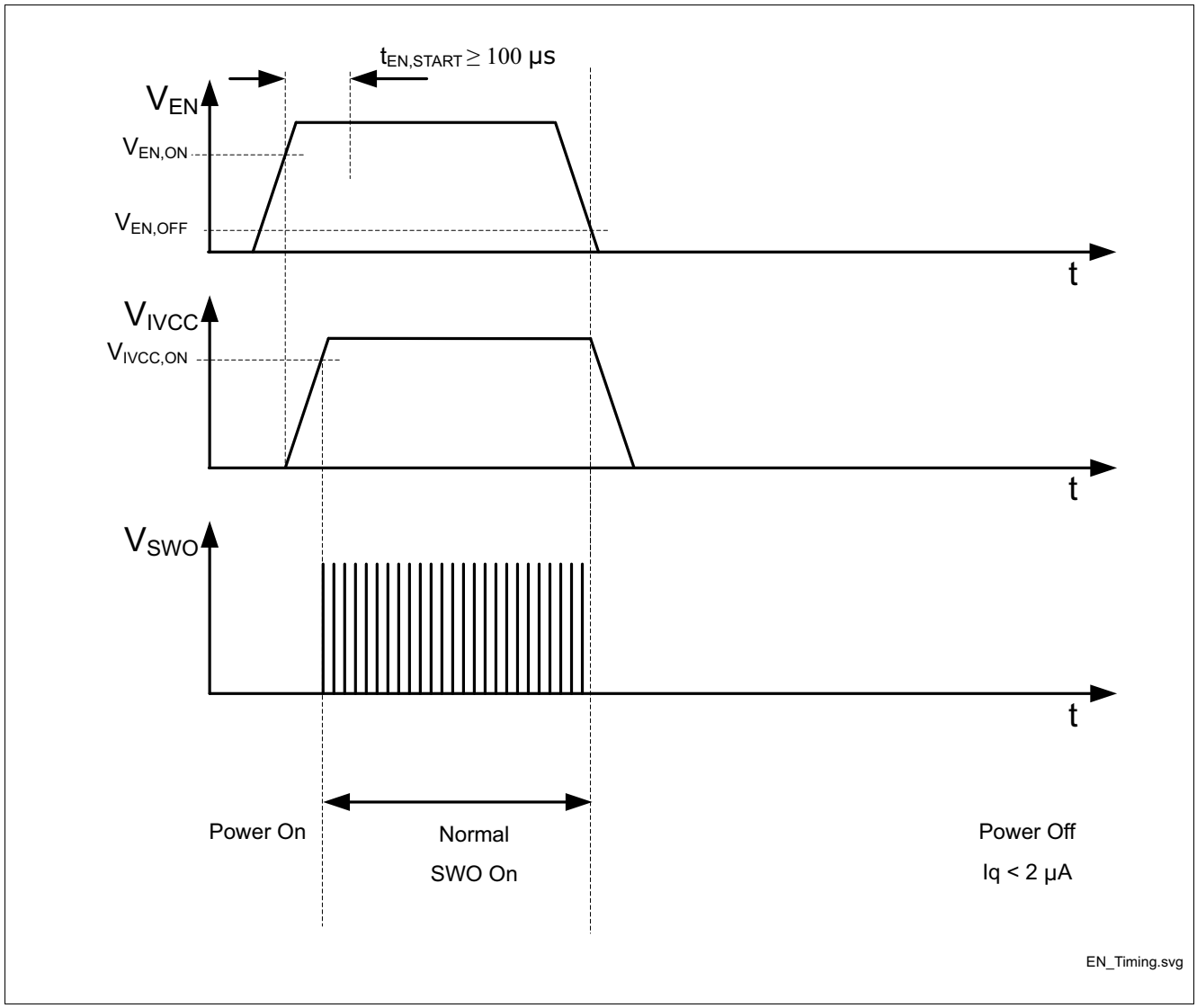



**Figure 6 Timing Diagram Enable**

## 7.2 Electrical Characteristics

$V_{IN}$ = 6V to 40V; $T_j$ = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| *Enable Input:* | | | | | | | |
| 7.2.1 | Enable Turn On Threshold | $V_{EN,ON}$ | 3.0 | – | | V | – |
| 7.2.2 | Enable Turn Off Threshold | $V_{EN,OFF}$ | – | – | 0.8 | V | – |
| 7.2.3 | Enable Hysteresis | $V_{EN,HYS}$ | 50 | 200 | 400 | mV | – |
| 7.2.4 | Enable High Input Current | $I_{EN,H}$ | – | – | 30 | µA | $V_{EN}$ = 16.0 V |
| 7.2.5 | Enable Low Input Current | $I_{EN,L}$ | – | 0.1 | 1 | µA | $V_{EN}$ = 0.5 V |
| 7.2.6 | Enable Startup Time[1)] | $t_{EN,START}$ | 100 | – | – | µs | – |
| *Current Consumption* | | | | | | | |
| 7.2.7 | Current Consumption, Shutdown Mode | $I_{q\_off}$ | – | – | 2 | µA | $V_{EN}$ = 0.8 V; $T_j \leq$ 105C; $V_{IN}$ = 16V |
| 7.2.8 | Current Consumption, Active Mode[2)] | $I_{q\_on}$ | – | – | 7 | mA | $V_{EN} \geq$ 4.75 V; $I_{BO}$ = 0 mA; $V_{IN}$ = 16V $V_{SWO}$ = 0% Duty |

1) Not subject to production test, specified by design.

2) Dependency on switching frequency and gate charge of boost.

# 8 Linear Regulator

## 8.1 Description

The internal linear voltage regulator supplies the internal gate drivers with a typical voltage of 5 V and current up to 50 mA. An external output capacitor with low ESR is required on pin IVCC for stability and buffering transient load currents. During normal operation the external boost MOSFET switch will draw transient currents from the linear regulator and its output capacitor. Proper sizing of the output capacitor must be considered to supply sufficient peak current to the gate of the external MOSFET switch. Please refer to application section for recommendations on sizing the output capacitor. An integrated power-on reset circuit monitors the linear regulator output voltage and resets the device in case the output voltage falls below the power-on reset threshold. The power-on reset helps protect the external switches from excessive power dissipation by ensuring the gate drive voltage is sufficient to enhance the gate of an external logic level n-channel MOSFET.

IVCC stays at around 300 mV when Enable signal is off. No external circuit should be connected to IVCC

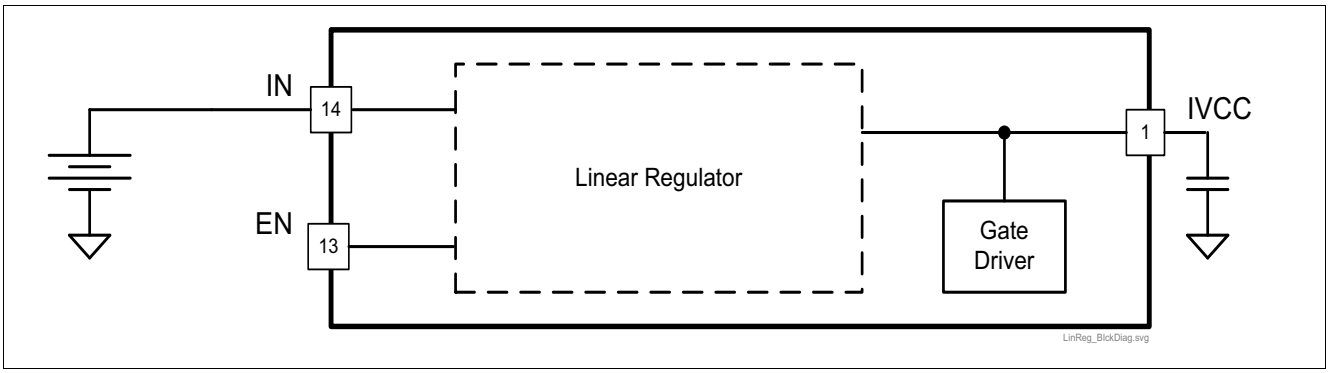



**Figure 7 Voltage Regulator Block Diagram and Simplified Application Circuit**

## 8.2 Electrical Characteristics

$V_{IN}$ = 6V to 40V; $T_j$ = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| 8.2.1 | Output Voltage | $V_{IVCC}$ | 4.6 | 5 | 5.4 | V | 6 V ≤ $V_{IN}$ ≤ 45 V<br>0.1 mA ≤ $I_{IVCC}$ ≤ 50 mA |
| 8.2.2 | Output Current Limitation | $I_{LIM}$ | 51 | | 110 | mA | $V_{IN}$ = 13.5 V<br>$V_{IVCC}$ = 4.5V |
| 8.2.3 | Drop out Voltage | $V_{DR}$ | | | 1000 | mV | $I_{IVCC}$ = 50mA [1] |
| 8.2.4 | Output Capacitor | $C_{IVCC}$ | 0.47 | | 3 | µF | [2] |
| 8.2.5 | Output Capacitor ESR | $R_{IVCC,ESR}$ | | | 0.5 | Ω | $f$ = 10kHz |
| 8.2.6 | Undervoltage Reset Headroom | $V_{IVCC,HDRM}$ | 100 | – | – | mV | $V_{IVCC}$ decreasing<br>$V_{IVCC}$ - $V_{IVCC,RTH,d}$ |
| 8.2.7 | Undervoltage Reset Threshold | $V_{IVCC,RTH,d}$ | 4.0 | – | – | V | $V_{IVCC}$ decreasing |
| 8.2.8 | Undervoltage Reset Threshold | $V_{IVCC,RTH,i}$ | – | – | 4.5 | V | $V_{IVCC}$ increasing |

1) Measured when the output voltage $V_{CC}$ has dropped 100 mV from its nominal value.

2) Minimum value given is needed for regulator stability; application might need higher capacitance than the minimum.

# 9 Protection and Diagnostic Functions

## 9.1 Description

T

he TLE8386-2EL has integrated circuits to protect against output overvoltage, open feedback and overtemperature faults. During an overvoltage the gate driver outputs SWO will turn off. In the event of an overtemperature condition the integrated thermal shutdown function turns off the gate drivers and internal linear voltage regulator. If the connection from pin FB to the output voltage resistor divider should be lost, an internal current source connected to Pin FB will draw the voltage above this limit and shut the external MOSFET off. The typical junction shutdown temperature is 175°C. After cooling down the IC will automatically restart operation. Thermal shutdown is an integrated protection function designed to prevent immediate IC destruction and is not intended for continuous use in normal operation.

## 9.2 Electrical Characteristics

$V_{IN}$ = 6V to 40V; $T_j$ = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| *Temperature Protection:* | | | | | | | |
| 9.2.1 | Over Temperature Shutdown | $T_{j,SD}$ | 160 | 175 | 190 | °C | – |
| 9.2.2 | Over Temperature Shutdown Hystereses | $T_{j,SD,HYST}$ | – | 15 | – | °C | – |
| *Overvoltage Protection:* | | | | | | | |
| 9.2.3 | Output Over Voltage Feedback Threshold Increasing | $V_{OVFB,TH}$ | 8 | 10 | 12 | % | 10% higher of regulated voltage |
| 9.2.4 | Output Over Voltage Feedback Hysteresis | $V_{OVFB,HYS}$ | | 5 | | % | Output Voltage decreasing |
| 9.2.5 | Over Voltage Reaction Time | $t_{OVPRR}$ | 2 | – | 10 | µs | Output Voltage decreasing |

*Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

# 10 Application Information

*Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

## 10.1 Boost Converter Application Circuit

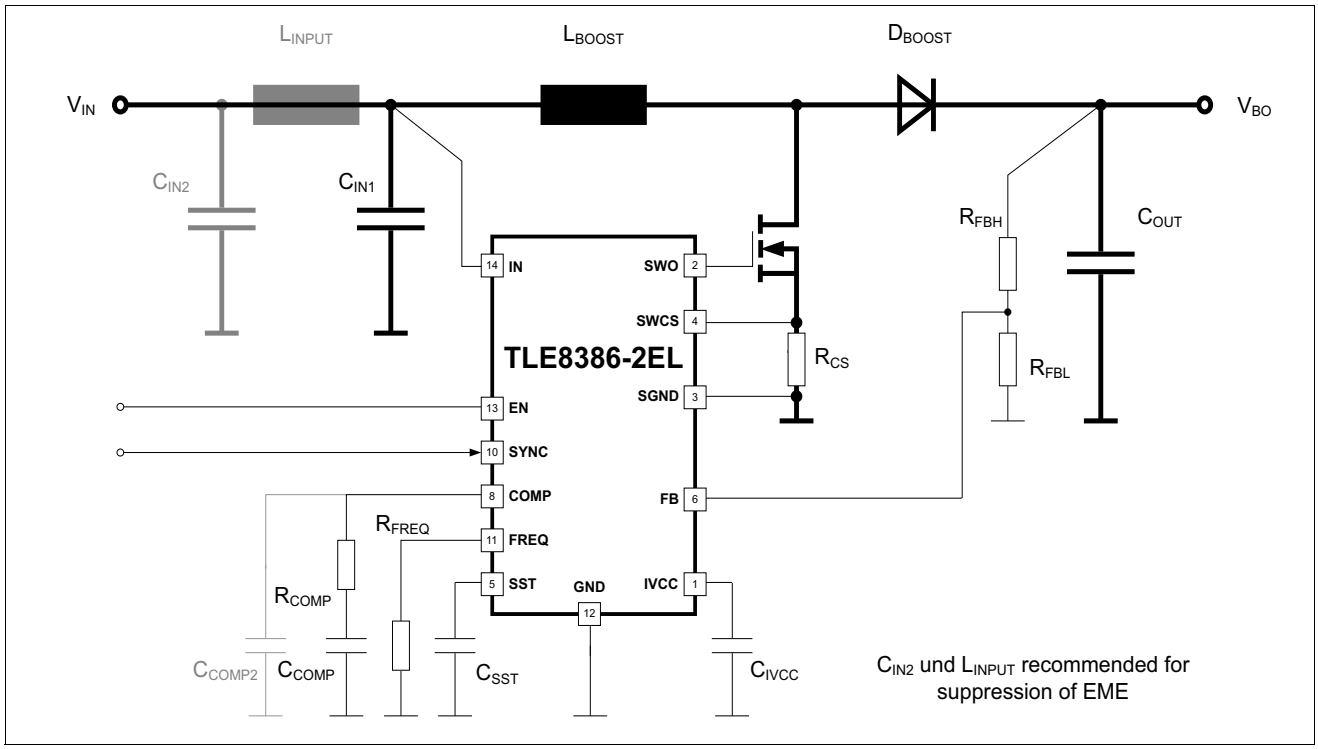



**Figure 8 Boost Converter Application Circuit**

| Reference Designator | Value | Manufacturer | Part Number | Type | Quantity |
|---|---|---|---|---|---|
| $D_{BOOST}$ | Schottky, 3 A, 100 $V_R$ | Vishay | SS3H10 | Diode | 1 |
| $C_{IN1}$, $C_{OUT}$ | 100 uF, 50V | Panasonic | EEEFK1H101GP | Capacitor | 2 |
| $C_{COMP}$ | 10 nF | TBD | TBD | Capacitor | 1 |
| $C_{IVCC}$ | 100 uF, 6.3V | Panasonic | EEFHD0J101R | Capacitor | 1 |
| $IC_1$ | -- | Infineon | TLD5095 | IC | 1 |
| $IC_2$ | -- | Infineon | XC886 | IC | 1 |
| $L_{BOOST}$ | 100 uH | Coilcraft | MSS1278T-104ML_ | Inductor | 1 |
| $R_{COMP}$ | 10 kΩ | TBD | TBD | Resistor | 1 |
| $C_{SST}$ | 2.2 nF | TBD | TBD | Capacitor | 1 |
| $R_{FREQ}$ | 20 kΩ, 1% | Panasonic | ERJ3EKF2002V | Resistor | 1 |
| $R_{FBH}$ | 11 kΩ, 1% | Panasonic | ERJ3EKF1102V | Resistor | 1 |
| $R_{FBL}$ | 1 kΩ, 1% | Panasonic | ERJ3EKF1001V | Resistor | 1 |
| $R_{CS}$ | 50 mΩ, 1% | Panasonic | ERJB1CFR05U | Resistor | 1 |

**Figure 9 Boost Application Circuit Bill of Material**

*Note: This is a simplified example of an application circuit. The function must be verified in the real application.*

### 10.1.1 Principle:

The TLE8386-2EL can be configured as a boost converter, where the desired output voltage $V_{BO}$ is always higher than the input voltage $V_{IN}$. A boost convertor is not short-circuit protected. If the output voltage $V_{BO}$ is shorted, the output current will only be limited by the input voltage $V_{IN}$ capability.

A typical boost converter application is shown in **Figure 8**, the elements and abbreviations and their meanings are:

- $L_{BOOST}$ = boost inductor
- $L_{INPUT}$ = input filter inductor, recommended to reduce electromagnetic emissions
- $C_{IN1}$ = input filter capacitor
- $C_{IN2}$ = additional input filter capacitor, recommended to reduce electromagnetic emissions
- $C_{OUT}$ = output filter capacitor
- $D_{BOOST}$ = output diode
- $V_{IN}$ = input voltage
- $V_{INMIN}$ = minimum input voltage
- $V_{BO}$ = boost output voltage
- $R_{CS}$ = current sense resistor
- $R_{FBH}$ = boost output voltage resistor divider, highside resistor
- $R_{FBL}$ = boost output voltage resistor divider, lowside resistor
- $R_{COMP}$, $C_{COMP}$ = compensation network elements
- $R_{FREQ}$ = frequency setting resistor
- $C_{SST}$ = softstart setting capacitor
- $C_{IVCC}$ = capacitor for internal LDO
- D = duty cycle
- $D_{MAX}$ = maximum duty cycle
- $f_{FREQ}$ = Switching Frequency
- $I_{IN}$ = input current
- $I_{BO}$ = output current
- $I_{BOMAX}$ = maximum output current

The ratio between input voltage $V_{IN}$ and output voltage $V_{BO}$ in continuos conduction mode (CCM) is:

$$\frac{V_{BO}}{V_{IN}} = \frac{1}{1-D} \Leftrightarrow D = \frac{V_{BO}-V_{IN}}{V_{BO}}$$

In discontinous conduction mode (DCM) the conversion ratio at a fixed frequency is higher, the switching current increases and efficiency is reduced. The maximum duty cycle $D_{MAX}$ occurs for minimum input voltage $V_{INMIN}$.

### 10.1.2 Component Selection:

**Power MOSFET selection:**

The important parameters for the choice of the power MOSFET are:

- Drain-source voltage rating $V_{DS}$: The power MOSFET will see the full output voltage $V_{BO}$ plus the output diode ($D_{BOOST}$) forward voltage. During its off-time additional ringing across drain-to-source will occur.
- On-resistance $R_{DSON}$ for efficiency reasons and power dissipation
- Maximum drain current $I_{DMAX}$
- Gate-to-source charge and gate-to-drain charge
- Thermal resistance

It is recommended to choose a power MOSFET with a drain-source voltage rating $V_{DS}$ of at least 10 V higher than the output voltage $V_{BO}$.

The power dissipation $P_{LOSSFET}$ in the power MOSFET can be calculated using the following formula:

- $C_{RSS}$ = reverse transfer capacitance, please refer to power MOSFET data sheet
- $I_{BOOSTMAX}$ = maximum average current through the boost inductor $L_{BOOST}$.

$$P_{LOSSFET} = I_{BOOSTMAX}^{2} \times R_{DSON} + 2 \times V_{BO}^{2} \times I_{BOOSTMAX} \times C_{RSS} \times \frac{f_{FREQ}}{1A}$$

The first term in the equation above gives the conduction losses in the power MOSFET, the second term the switching losses. To optimize the efficiency, $R_{DSON}$ and $C_{RSS}$ should be minimized.

**Current sense resistor $R_{CS}$ selection:**

For control and protection, the TLE8386-2EL measures the power MOSFET current by a current sense resistor $R_{CS}$, which is located between the power MOSFET source and ground. For proper function it is very important:

- To locate the current sense resistor as close as possible to the TLE8386-2EL
- To use short (low resistive and low inductive) traces between the power MOSFET source and ground.
- To use short (low resistive and low inductive) traces between the current sense resistor $R_{CS}$ highside and lowside and the pins SWCS and SGND (it is not recommended to use pin GND instead of pin SGND for power MOSFET current measurement).
- The value of $R_{CS}$ should be selected to make sure that the maximum peak sense voltage $V_{SENSEPEAK}$ during steady state normal operation will be lower than the adjusted current limit threshold (current limit function!). It is recommended to give a 20% margin.
- The value of $R_{CS}$ should be selected to make sure that the power MOSFET maximum drain current $I_{DMAX}$ will not be exceeded (please refer to power MOSFET data sheet).

The figure below shows the voltage waveform over the current sense resistor $R_{CS}$ during a switching cycle:

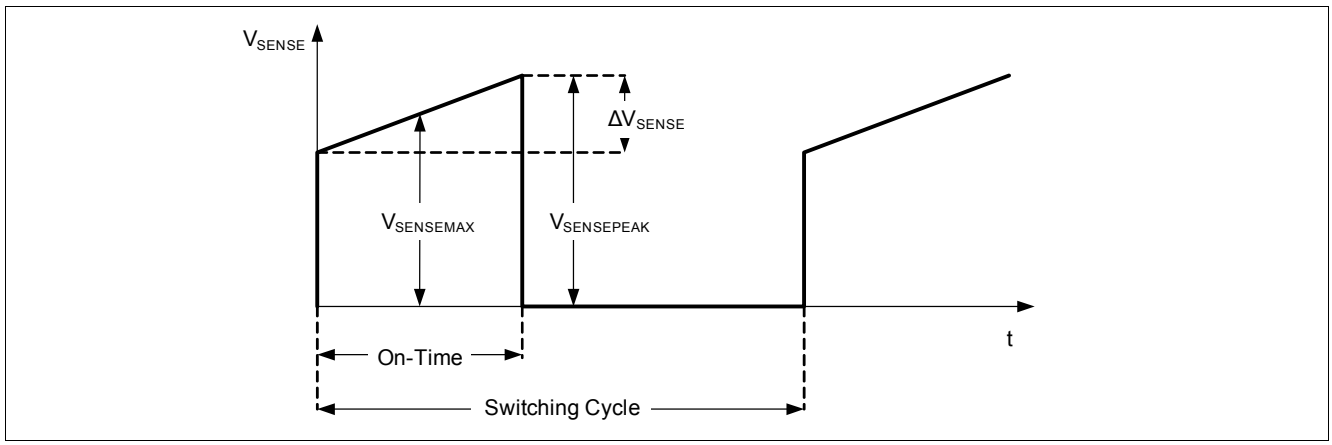



**Figure 10 Sense voltage $V_{SENSE}$ waveform during a switching cycle**

- $V_{SENSEMAX}$ = maximum average sense voltage at maximum output current $I_{BO}$ measured during on-time.
- $V_{SENSEPEAK}$ = maximum peak sense voltage at maximum output current $I_{BO}$ at end of on-time.
- $\Delta V_{SENSE}$ = ripple voltage across $R_{CS}$ (switch ripple current) during on-time, represents the peak-to-peak ripple current in the boost inductor $L_{BOOST}$.

The maximum (peak-to-peak) switch current ripple percentage $\chi$ (will be needed for further calculations of inductor values) can be calculated considering the 20% margin by following equation:

$$\chi = \frac{\Delta V_{SENSE}}{0{,}80 \times V_{SWCS} - 0{,}50 \times \Delta V_{SENSE}}$$

- $V_{SWCS}$ = Switch peak over current threshold
- $\chi$ is recommended to fall in the range between 0.2 to 0.6 (please refer to calculations in the following chapters)

The value of the sense resistor $R_{CS}$ can be calculated as follows:

$$R_{CS} = \frac{0{,}80 \times V_{SWCS}}{I_{BOOSTPEAK}}$$

- $I_{BOOSTPEAK}$ = peak current through the boost inductor $L_{BOOST}$ (will be calculated at boost inductor selection)

**Boost inductor $L_{BOOST}$ selection:**

The important parameters for selecting the boost inductor are:

- Inductor $L_{BOOST}$
- Maximum RMS current rating $I_{BOOSTRMS}$ for thermal design
- Saturation current threshold $I_{BOOSTSAT}$

The maximum average inductor current is:

$$I_{BOOSTMAX} = I_{BOMAX} \times \frac{1}{1 - D_{MAX}}$$

The ripple current through the boost inductor is:

$$\Delta I_{BOOST} = \chi \times I_{BOOSTMAX} = \chi \times I_{BOMAX} \times \frac{1}{1 - D_{MAX}}$$

The peak current through the boost inductor is:

$$I_{BOOSTPEAK} = I_{BOOSTMAX} \times \left(1 + \frac{\chi}{2}\right) < I_{BOOSTSAT}$$

(The peak current trough the boost inductor must be smaller than the saturation current threshold!)

The RMS current through the boost inductor is:

$$I_{BOOSTRMS} = I_{BOOSTMAX} \times \sqrt{1 + \frac{\chi^2}{12}}$$

The boost inductor value $L_{BOOST}$ can be calculated by the following equation:

$$L_{BOOST} = \frac{V_{INMIN}}{\Delta I_{BOOST} \times f_{FREQ}} \times D_{MAX}$$

In fixed frequency mode an external resistor determines the switching frequency. The minimum boost inductor for fixed frequency is given by the formula below:

- $L_{BOOSTMIN}$ = minimum Inductance required (minimum value of $L_{BOOST}$)

$$L_{BOOSTMIN} \geq \frac{V_{BO}[V] \times R_{CS}[\Omega]}{106 \times 10^{-3}[V] \times f_{FREQ}[Hz]}$$

Following the previous equations the user should choose the boost inductor having sufficient saturation and RMS current ratings.

The boost inductor value influences the current ripple $\Delta I_{BOOST}$:

- A larger boost inductor value decreases the current ripple $\Delta I_{BOOST}$, but reduces also the current loop gain.
- A lower boost inductor value increases the current ripple $\Delta I_{BOOST}$, but provides faster transient response. A lower boost inductor value also results in higher input current ripple and greater core losses.

**Output diode $D_{BOOST}$ selection:**

Guidelines to choose the diode:

- Fast switching diode
- Low forward drop
- Low reverse leakage current
- It is recommended to choose the repetitive reverse voltage rating $V_{RRM}$ (please refer to diode data sheet) at least 10V higher than the boost converter output voltage $V_{BO}$.

The average forward current in normal operation is equal to the boost converter output current $I_{BO}$ and the peak current through the diode $I_{DPEAK}$ (occurs in off-time of the power MOSFET) is:

$$I_{DPEAK} = I_{BOOSTPEAK} = I_{BOOSTMAX} \times \left(1 + \frac{\chi}{2}\right)$$

The power dissipation $P_{LOSSDIO}$ in the output diode $D_{BOOST}$ is:

$$P_{LOSSDIO} = I_{BOMAX} \times V_D$$

- $V_D$ = forward drop voltage of diode $D_{BOOST}$ (please refer to diode data sheet).

**Output filter capacitor $C_{OUT}$ selection:**

Choosing the correct output capacitor for given output ripple voltage, the influence of

- ESR = equivalent series resistance,
- ESL = equivalent series inductance and
- bulk capacitance have to be considered.

The effects of these three parameters is additional ringing on the output voltage $V_{BO}$.

The voltage ripple at the output voltage $V_{BO}$ depends on:

- $\Delta V_{ESR}$: in percent, related to the ESR of the output capacitor(s)
- $\Delta V_{COUT}$: in percent, related to the bulk capacitance of the output capacitor(s)
- To receive the total voltage ripple, the influence of $\Delta V_{ESR}$ and $\Delta V_{COUT}$ must be counted together.

The output capacitor can be calculated using the following equation (which contains the influence of the bulk capacitance on the output voltage ripple):

$$C_{OUT} \geq \frac{I_{BOMAX}}{\Delta V_{COUT} \times V_{OUT} \times f_{FREQ}}$$

Influence of the capacitor ESR on the output voltage ripple:

$$ESR_{COUT} \leq \frac{\Delta V_{ESR}}{I_{DPEAK}}$$

The output capacitor experiences high RMS ripple currents, the RMS ripple current rating can be determined using the following formula:

$$I_{COUTRMS} \geq I_{BOMAX} \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}}$$

- $I_{COUTRMS}$ = RMS ripple current rating at switching frequency $I_{FREQ}$.

To meet the ESR requirements often multiple capacitors are paralleled. Typically, once the ESR requirement is met, the output capacitance is adequate for filtering and has the required RMS current rating. Additional ceramic capacitors are commonly used to reduce the effects of parasitic inductance to reduce high frequent switching noise on the boost converter output.

**Input filter capacitor $C_{IN1}$ selection:**

The input filter capacitor $C_{IN1}$ has to compensate the alternate current content or current ripple on the input line, recommended values are from 10µF to 100µF, to improve the suppression of high frequent distortions a parallel ceramic capacitor might be necessary.

The RMS input capacitor ripple current $I_{IN1RMS}$ for a boost converter is:

$$I_{IN1RMS} = 0{,}30 \times \Delta I_{BOOST}$$

**Compensation network elements $R_{COMP}$, $C_{COMP}$ selection:**

To compensate the feedback loop of the TLE8386-2EL a series network of $R_{COMP}$, $C_{COMP}$ is usually connected from pin COMP to ground. For most applications the capacitor $C_{COMP}$ should be in the range of 470pF to 22nF, and the resistor $R_{COMP}$ should be in the range of 5kΩ to 100kΩ. An additional capacitor $C_{COMP2}$ might be usefull to improve stability. $C_{COMP}$ and $C_{COMP2}$ should be a low ESR ceramic capacitors.

A practical approach to determine the compensation network is to start with the application circuit as shown in the data sheet and tune the compensation network to optimize the performance. Stability of the loop should then be checked under all operating conditions, including output current and variations and over the entire temperature range.

**Output boost voltage $V_{BO}$ adjustment by determining the output voltage resistor divider $R_{FBH}$, $R_{FBL}$:**

- $V_{FB}$ = feedback reference voltage

$$V_{BO} = V_{FB} \times \frac{R_{FBH} + R_{FBL}}{R_{FBL}}$$

($V_{BO}$ is always higher than $V_{IN}$ during operation of the boost converter)

**Additional input filter inductor $L_{INPUT}$ and capacitor $C_{IN2}$ selection:**

- $f_{FILTER}$ = resonance frequency of the additional input filter

The input filter inductor $L_{INPUT}$ should have a saturation current value equal to $L_{BOOST}$, capacitor $C_{IN2}$ should be a low ESR ceramic capacitor. Both elements are forming a low pass filter to suppress conducted disturbances on the $V_{IN}$ line. To obtain an optimum suppression, the input filter resonance frequency $f_{FILTER}$ should be at least ten times lower than the switching frequency $f_{FREQ}$:

$$f_{FREQ} > 10 \times \left( f_{FILTER} = \frac{1}{2\Pi\sqrt{L_{INPUT} \times C_{IN2}}} \right)$$

The use of an additional input filter is depending on the requirements of the application.

For selection of $R_{FREQ}$, $C_{SST}$ and $C_{IVCC}$ please refer to previous chapters.

## 10.2 Further Information on TLE8386-2EL

### 10.2.1 General Layout recommendations

**Introduction:**

A boost converter is a potential source of electromagnetic disturbances which may affect the environment as well as the device itself and cause sporadic malfunction up to damages depending on the amount of noise.

In principal we may consider the following basic effects:

- Radiated magnetic fields caused by circular currents, occurring mostly with the switching frequency and their harmonics
- Radiated electric fields, often caused by (voltage) oscillations
- Conducted disturbances (voltage spikes or oscillations) on the lines, mostly input and output lines.

**Radiated magnetic fields:**

Radiated magnetic fields are caused by circular currents occurring in so called “current windows”. These circular currents are alternating currents which are driven by the switching transistor. The alternating current in these windows are driving magnetic fields. The amount of magnetic emissions is mostly depending on the amplitude of the alternating current and the size of the so-called “window” (this is the area, which is defined by the circular current paths. We can divide into two windows:

- the input current “window” (path consisting of $C_{IN1}$, $L_{BOOST}$ and the power MOSFET): Only the alternate content of the input current $I_{IN}$ is considered.
- the output current “window”: (path consisting of the power MOSFET, $D_{BOOST}$ and $C_{OUT}$): Output current ripple $\Delta I$

The area of these “windows” has to be kept as small as possible, with the relating elements placed next to each others. It is highly recommended to use a ground plane as a single layer which covers the complete regulator area with all components shown in this figure. All connections to ground shall be as short as possible

**Radiated electric fields:**

Radiated electric fields are caused by voltage oscillations occurring due to stray inductances and stray capacitances at the connection between power MOSFET, output diode $D_{BOOST}$ and output capacitor $C_{OUT}$. They are also of course influenced by the commutation of the current from the power MOSFET to the output diode $D_{BOOST}$. Their frequencies might be between 10 and 100 MHz. Therefore it is recommended to use a fast Schottky diode and to keep the connections in this area as low inductive as possible. This can be achieved by using short and broad connections and to arrange the related parts as close as possible. Following the recommendation of using a ground layer these low inductive connections will form together with the ground layer small capacitances which are desirable to damp the slope of these oscillations. The oscillations use connections or wires as antennas, this effect can also be minimized by the short and broad connections.

**Conducted disturbances:**

Conducted disturbances are voltage spikes or voltage oscillations, occurring permanently or by occasion mostly on the input or output connections. Comparable to the radiated electric fields they are caused by voltage oscillations occurring due to stray inductances and stray capacitances at the connection between power MOSFET, output diode $D_{BOOST}$ and output capacitor $C_{OUT}$.

Their frequencies might be between 10 and 100 MHz. They are super positioned to the input and output voltage and might thus disturb other components of the application.

The countermeasures against conducted disturbances are similar to the radiated electric fields:

- it is recommended to use short an thick connections between the single parts of the converter
- all parts shall be mounted close together
- additional Filter capacitors (ceramic, with low ESR) in parallel to the output and input capacitor and as close as possible to the switching parts. Input and load current must be forced to pass these devices, do not connect them via thin lines. Recommended values from 10nF to 220nF
- for the input filter a so called “p” – Filter for maximum suppression might be necessary, which requires additional capacitors on the input

### 10.2.2 Additional information

- Please contact us for information regarding the Pin FMEA.
- and for existing application notes with more detailed information about the possibilities of this device
- For further information you may contact **http://www.infineon.com/**

# 11 Package Outlines

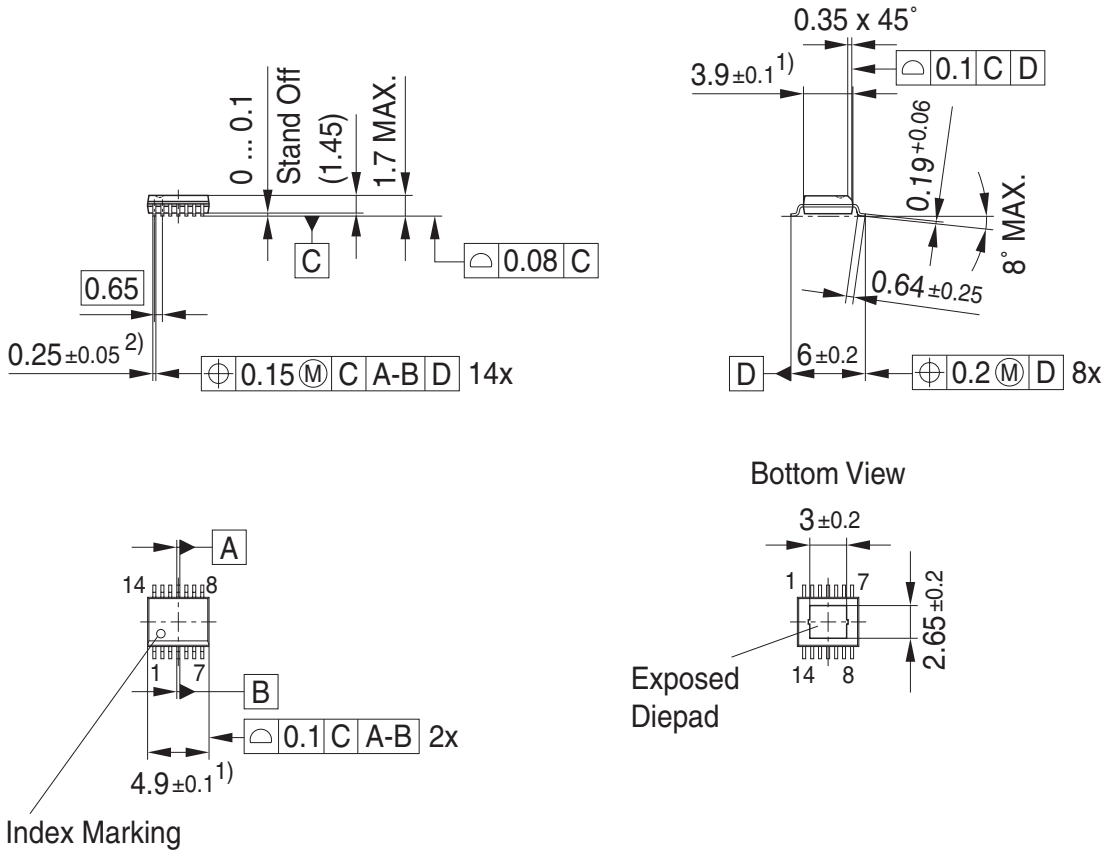



**Figure 11 PG-SSOP-14**

**Green Product (RoHS compliant)**

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further package information, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

# 12 Revision History

1.0

| Revision | Date | Changes |
|---|---|---|
| 1.0 | 2010-10-25 | Data Sheet |

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