

NTD6416ANL, NVD6416ANL

N-Channel Power MOSFET 100 V, 19 A, 74 mΩ

Features

- Low $R_{DS(on)}$
- High Current Capability
- 100% Avalanche Tested
- AEC-Q101 Qualified and PPAP Capable – NVD6416ANL
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	100	V
Gate-to-Source Voltage – Continuous	V_{GS}	± 20	V
Continuous Drain Current	Steady State	$T_C = 25^\circ\text{C}$	19
		$T_C = 100^\circ\text{C}$	13
Power Dissipation	Steady State	$T_C = 25^\circ\text{C}$	71
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	I_{DM}	70
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to +175	$^\circ\text{C}$
Source Current (Body Diode)	I_S	19	A
Single Pulse Drain-to-Source Avalanche Energy ($V_{DD} = 50 \text{ Vdc}$, $V_{GS} = 10 \text{ Vdc}$, $I_{L(pk)} = 18.2 \text{ A}$, $L = 0.3 \text{ mH}$, $R_G = 25 \Omega$)	E_{AS}	50	mJ
Lead Temperature for Soldering Purposes, 1/8" from Case for 10 Seconds	T_L	260	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Case (Drain) – Steady State	$R_{\theta JC}$	2.1	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	47	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

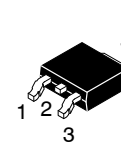
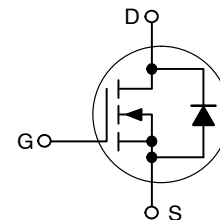
1. Surface mounted on FR4 board using 1 sq in pad size, (Cu Area 1.127 sq in [2 oz] including traces).



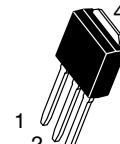
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$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
100 V	74 mΩ @ 10 V	19 A

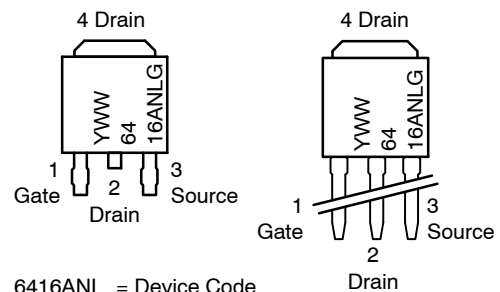


DPAK
CASE 369AA
STYLE 2



IPAK
CASE 369D
STYLE 2

MARKING DIAGRAM & PIN ASSIGNMENTS



6416ANL = Device Code
Y = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	100			V	
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			120		mV/°C	
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 100 V	T _J = 25°C			1.0	μA
			T _J = 125°C			10	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V				±100	nA

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250 μA	1.0		2.2	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J			5.4		mV/°C
Drain-to-Source On-Resistance	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 10 A		70	80	mΩ
		V _{GS} = 10 V, I _D = 10 A		62	74	
		V _{GS} = 10 V, I _D = 19 A		68	74	
Forward Transconductance	g _{FS}	V _{DS} = 5 V, I _D = 10 A		18		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 25 V		700	1000	pF	
Output Capacitance	C _{OSS}			110			
Reverse Transfer Capacitance	C _{RSS}			50			
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 80 V, I _D = 19 A		25	40	nC	
Threshold Gate Charge	Q _{G(TH)}			0.7			
Gate-to-Source Charge	Q _{GS}			2.4			
Gate-to-Drain Charge	Q _{GD}			9.6			
Plateau Voltage	V _{GP}			3.2			V
Gate Resistance	R _G			2.4			Ω

SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	t _{d(on)}	V _{GS} = 10 V, V _{DD} = 80 V, I _D = 19 A, R _G = 6.1 Ω		7.0		ns
Rise Time	t _r			16		
Turn-Off Delay Time	t _{d(off)}			35		
Fall Time	t _f			40		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 19 A	T _J = 25°C		0.9	1.2	V
			T _J = 125°C		0.72		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 19 A		50		ns	
Charge Time	T _a			38			
Discharge Time	T _b			14			
Reverse Recovery Charge	Q _{RR}			112			nC

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3. Switching characteristics are independent of operating junction temperatures.

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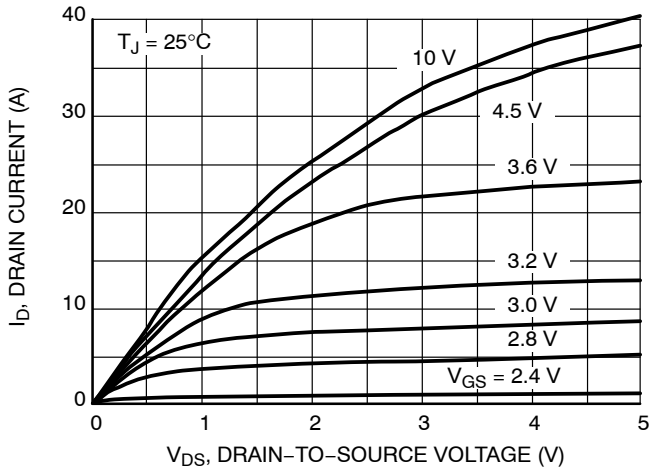


Figure 1. On-Region Characteristics

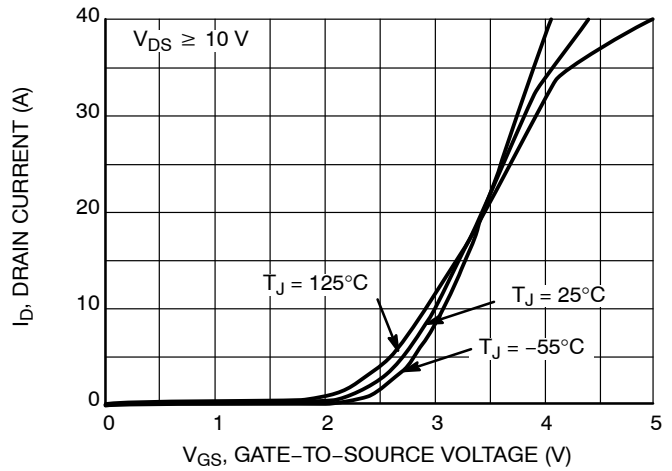


Figure 2. Transfer Characteristics

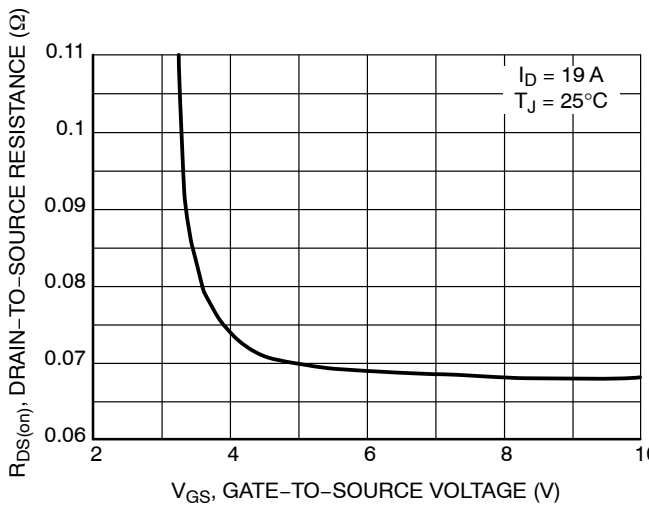


Figure 3. On-Region versus Gate-To-Source Voltage

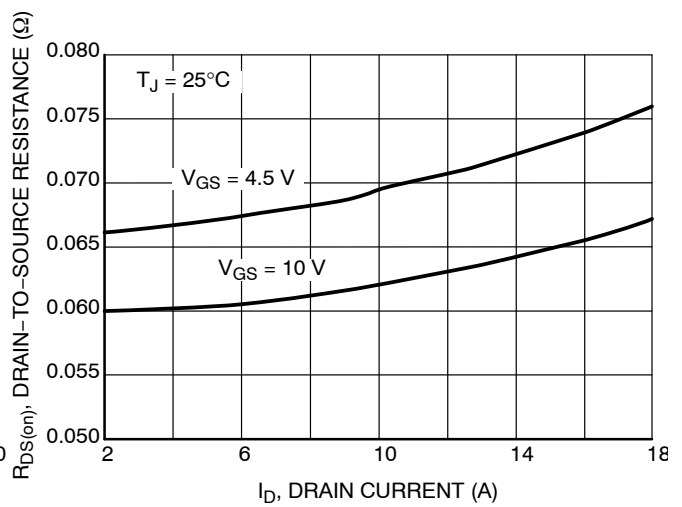


Figure 4. On-Region versus Drain Current and Gate-To-Source Voltage

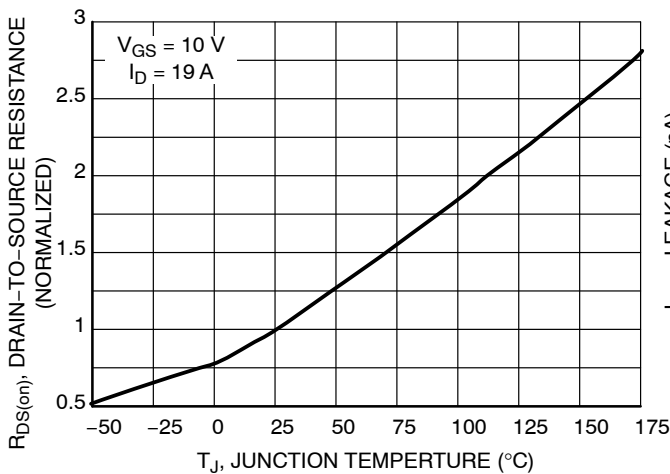


Figure 5. On-Resistance Variation with Temperature

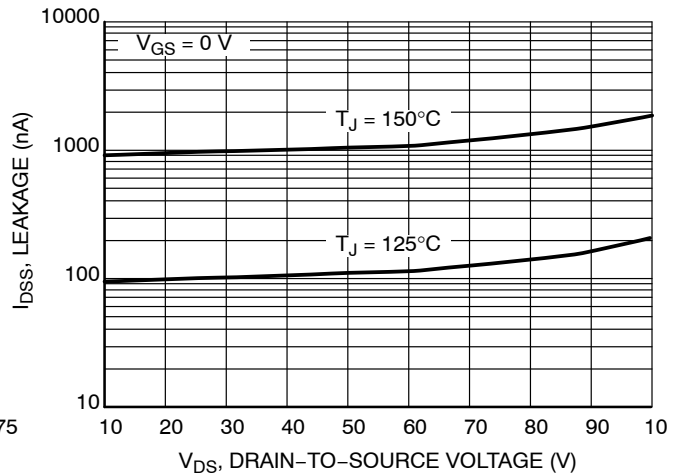


Figure 6. Drain-to-Source Leakage Current versus Voltage

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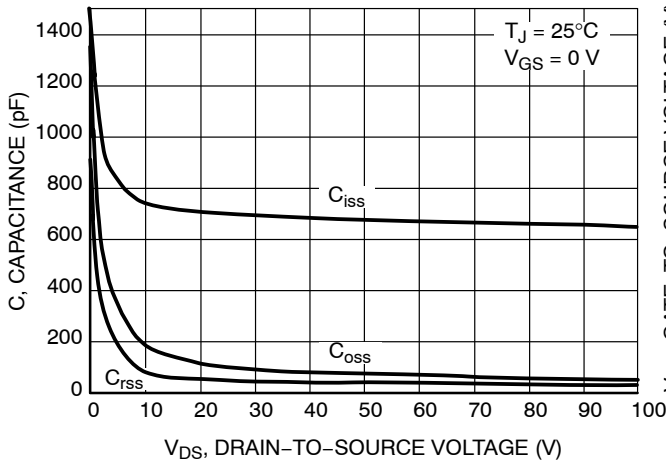


Figure 7. Capacitance Variation

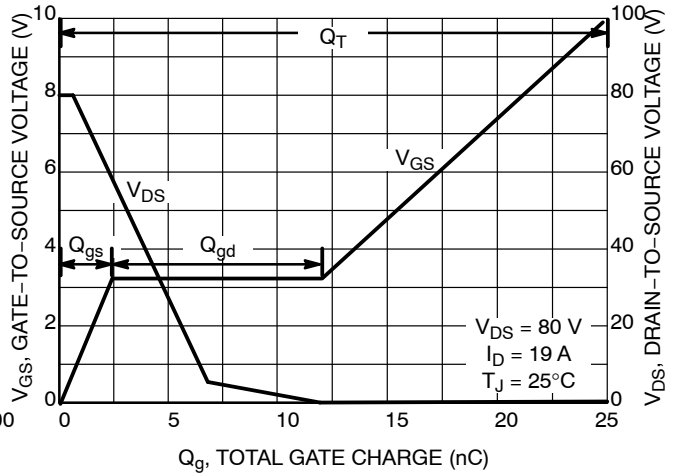


Figure 8. Gate-to-Source Voltage and Drain-to-Source Voltage versus Total Charge

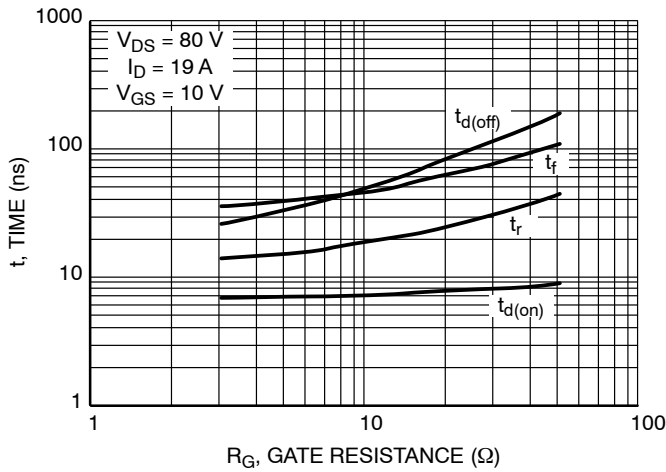


Figure 9. Resistive Switching Time Variation versus Gate Resistance

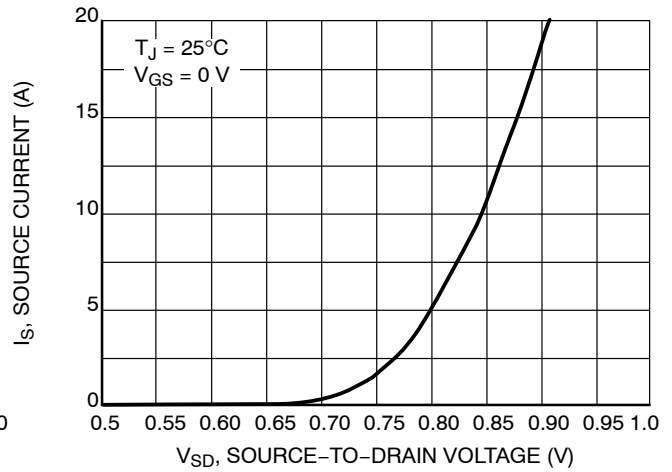


Figure 10. Diode Forward Voltage versus Current

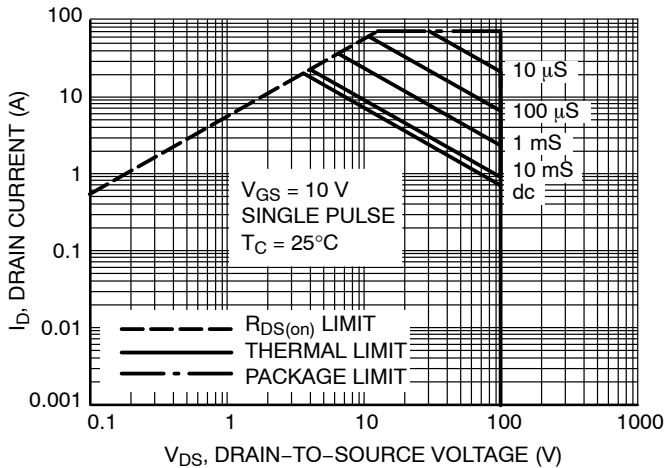


Figure 11. Maximum Rated Forward Biased Safe Operating Area

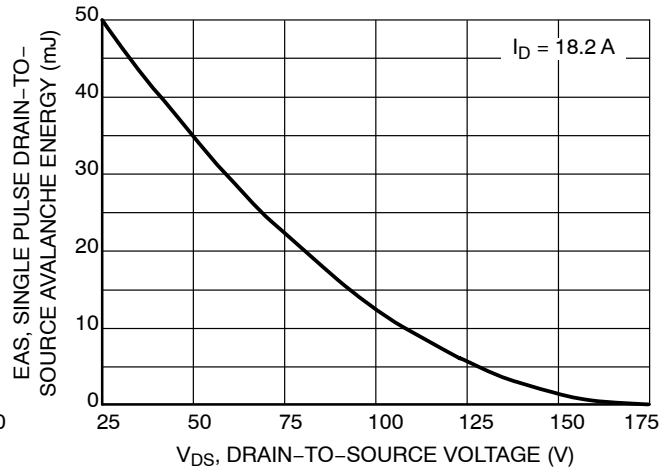


Figure 12. Resistive Switching Time Variation versus Gate Resistance

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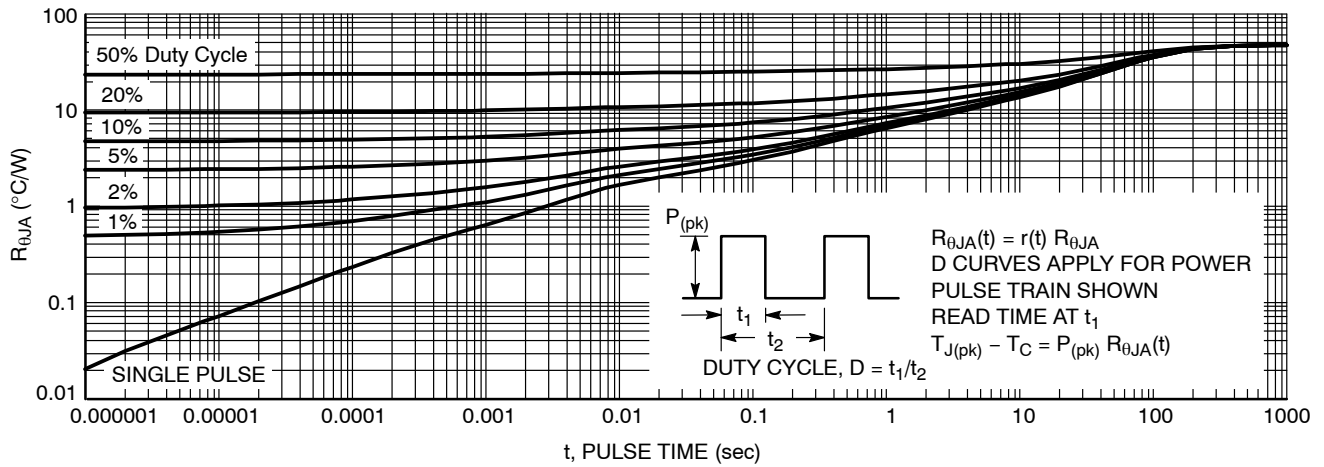


Figure 13. Thermal Response (NTD6416ANL DPAK PCB Cu Area 720 mm² PCB Cu thk 2 oz)

ORDERING INFORMATION

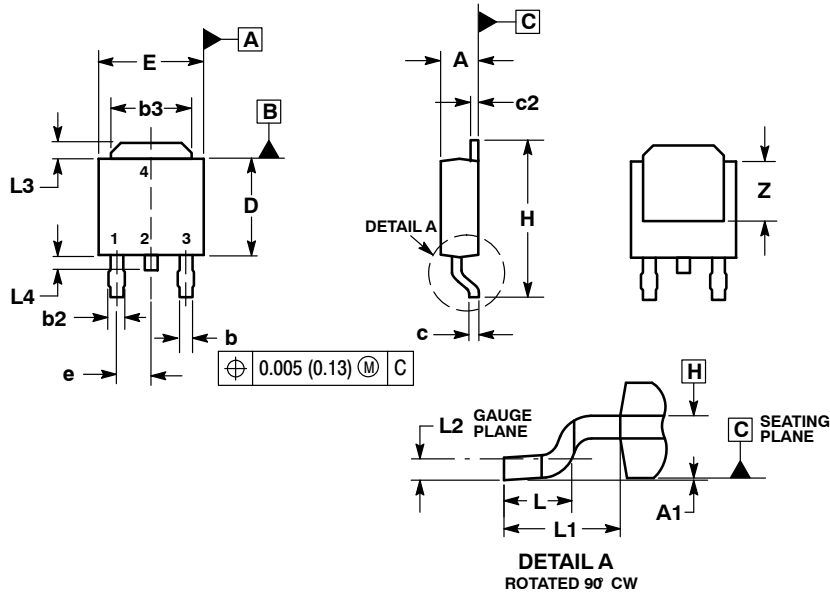
Device	Package	Shipping [†]
NTD6416ANLT4G	DPAK (Pb-Free)	2500 / Tape & Reel
NTD6416ANL-1G	IPAK (Pb-Free)	75 Units / Rail
NVD6416ANLT4G	DPAK (Pb-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTD6416ANL, NVD6416ANL

PACKAGE DIMENSIONS

DPAK (SINGLE GUAGE) CASE 369AA ISSUE B

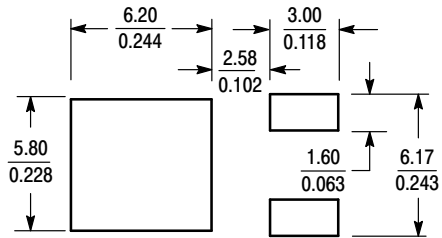


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

SOLDERING FOOTPRINT*



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

STYLE 2:

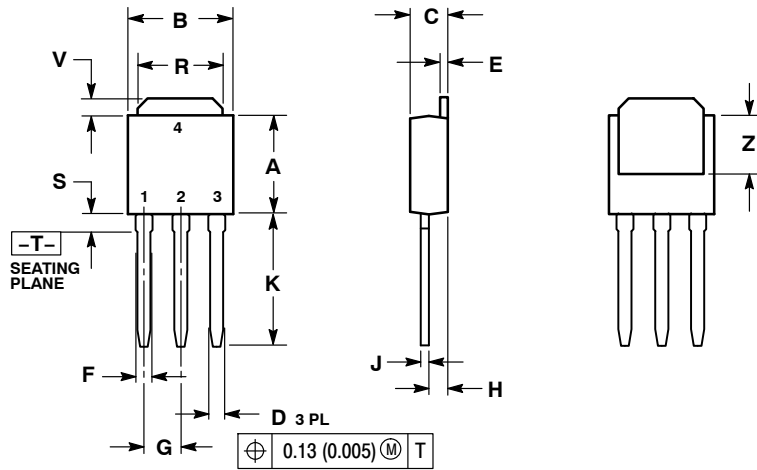
1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

IPAK CASE 369D ISSUE C




NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	BSC	2.29	BSC
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 2:

- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

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